Dual Synchronous Step-Down Controller with PMBus Interface

DESCRIPTION

The ES5201 is a dual output current mode synchronous step-down DC/DC controller with PMBus compliant serial interface. It operates over a wide input range from 4.5V to 42V. It includes two high speed differential remote sense amplifiers and provides accurate regulation for a variety of loads with an accurate 500mV±0.8% reference over full temperature range.

The ES5201 features programmable soft-start and power good indictors to simply power supply rail sequencing.

Its peak current mode control architecture provides cycle-by-cycle peak current protection and excellent line load regulation.

The DC/DC controller employs a unique fast transient architecture to achieve fast transient responses for high step-down applications. Both CCM and DCM operation are supported.

The ES5201 supports frequency synchronization and multi-phase/multi-IC Parallel Operation. Up to six ES5201s can be paralleled to deliver 300A current.

APPLICATIONS

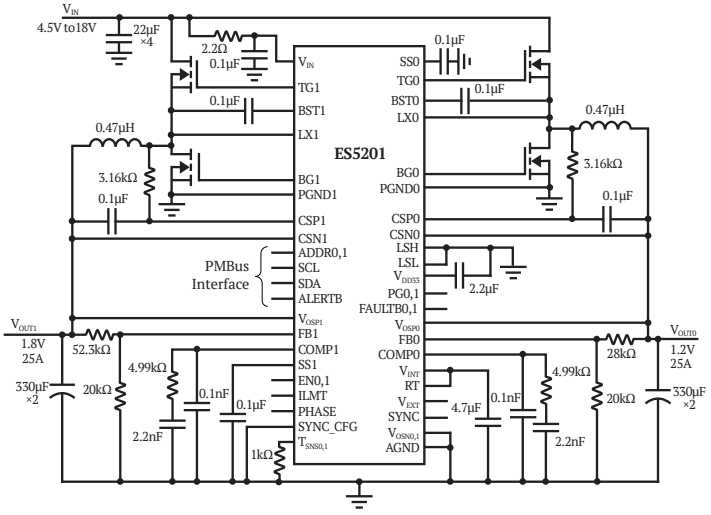
- Telecom, Server and Networking Systems
- DC Power Distribution System

FEATURES

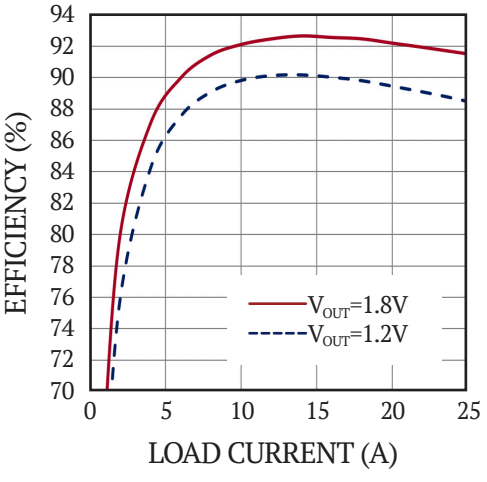
- Dual 180° Phased Controllers with Built in MOSFET Driver and Bootstrap Diode
- Wide Input Voltage Range 4.5V to 42V
- Output Voltage Range 0.5V to 5.5V
- High Efficiency: Up to 95%
- PMBus Compliant Serial Interface
  -Telemetry Read-Back V_{IN}, V_{OUT}, I_{OUT}, Temperature
  -Program V_{OUT}, OV/OC/OT Warning
- 0.5V±0.8% Voltage Reference Over -40°C to 125°C
- Dual True Differential Remote Sensing Amplifiers
- Selectable CCM or DCM Operation at Light Load
- Adjustable Fixed Frequency 200kHz to 1.3MHz
- $t_{ON(MIN)}$ = 60ns, Capable of Very Low Duty Cycles
- Programmable Soft-start with Output Pre-biased Function
- SYNC Input and Output for Up to 12-Phase Paralleling Operation
- Hiccup Mode for Overcurrent Protection
- Output Overvoltage Protection
- Power Good Indicator
- Available in 48-Lead 6mm × 6mm × 0.75mm QFN Package

TYPICAL APPLICATION

4.5V to 18V Input, Dual 25A Outputs DC/DC Regulator

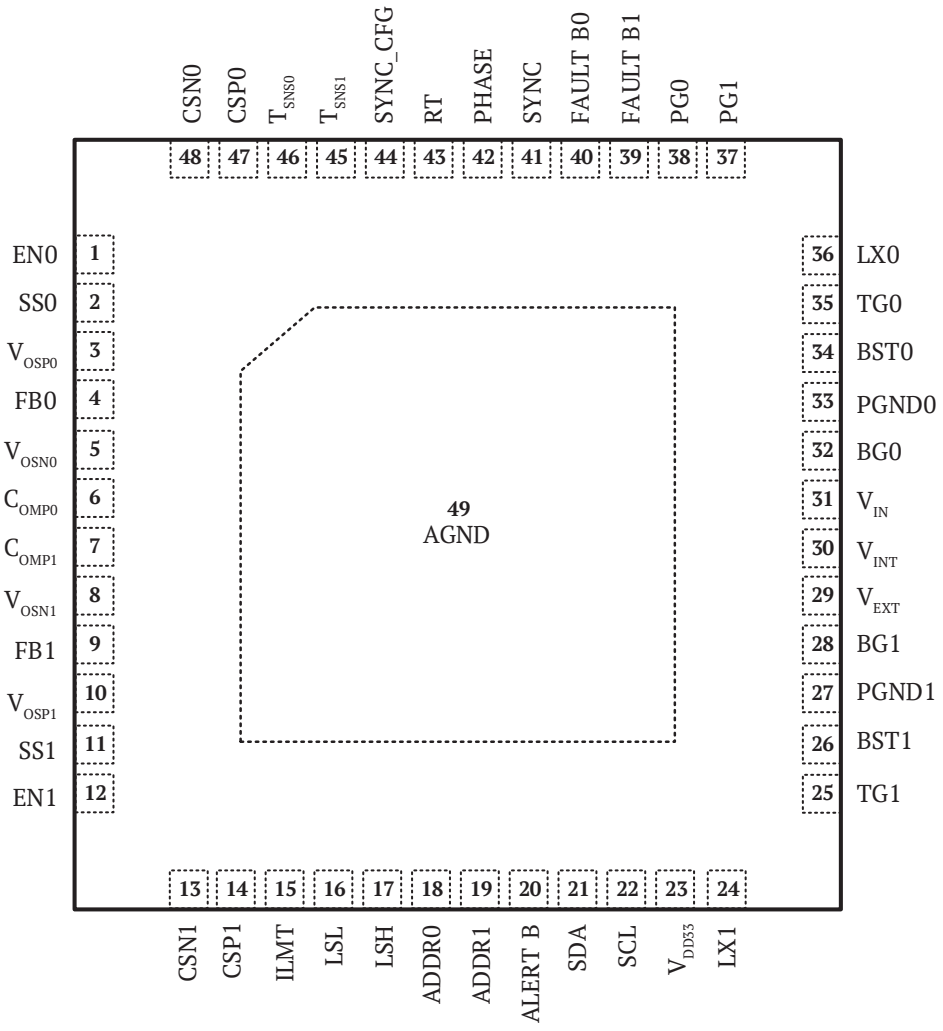


Efficiency at 12V Input Voltage



PIN CONFIGURATION AND FUNCTIONS

(TOP VIEW)



UJ PACKAGE
48-LEAD 6mm × 6mm × 0.75mm QFN PACKAGE
θ_{JA} = 31°C/W, θ_{JC} = 3°C/W

PIN#	PIN Name	PIN Description
1	EN0	Enable Pins. Pull low below 1.16V to disable the device and pull high above 1.22V to enable this device. There is a 1μA pull-up current for this pin. Once the EN pin rises above 1.22V, an additional 1μA pull-up current is added to the pin.
12	EN1	
2	SS0	External Soft-Start Voltage Pins. There is a 1μA pull-up current for this pin. Soft-start time can be adjusted by adding an appropriate external capacitor between this pin and AGND.
11	SS1	
3	V_{OSP0}	Positive Output Voltage Sense Input. Connect this pin to the positive side of the output voltage sense point.
10	V_{OSP1}	
4	FB0	Positive Inputs of Remote Sensing Amplifiers. Connect this pin to the external resistor divider across the output.
9	FB1	
5	V_{OSN0}	Negative Inputs of Remote Sensing Amplifiers. Connect this pin directly to the negative side of the output voltage sense point.
8	V_{OSN1}	
6	COMP0	Current Control Threshold and Error Amplifier Compensation Pins. The current comparators' threshold increases with this pin.
7	COMP1	
49	AGND	Analog Ground Pin.
13	CSN1	Current Comparator Negative Inputs. The negative input to the current comparator is connected to the output.
48	CSN0	
14	CSP1	Current Comparator Positive Inputs. The positive input to the current comparator is connected to DCR sensing network or current sense resistor.
47	CSP0	
15	ILMT	Current Comparators' Sense Voltage Range Select Pin. A resistor divider between V_{DD33} and AGND to this pin to set five different maximum current sense thresholds.
16	LSL	Inductor DCR Value Select Pin. A resistor divider between V_{DD33} and AGND to this pin to set 4 LSB bits of both channel's IOUT_CAL_GAIN value.
17	LSH	Inductor DCR Value Select Pin. A resistor divider between V_{DD33} and AGND to this pin to set 4 MSB bits of both channel's IOUT_CAL_GAIN value.
18	ADDR0	PMBus Address Select Pin. A resistor divider between V_{DD33} and AGND to this pin to set the 4 LSB PMBus address.
19	ADDR1	PMBus Address Select Pin. A resistor divider between V_{DD33} and AGND to this pin to set the 3 MSB PMBus address.
20	ALERTB	PMBus Alert Pin. A pull-up resistor is required for this open drain output pin.
21	SDA	Serial Bus Data Input and Open-Drain Output. A pull-up resistor is required in the application.
22	SCL	Serial Bus Clock Pin.
23	V_{DD33}	Internal 3.3V LDO Output. Decouple this pin to AGND with a minimum of 1μF low ESR ceramic or tantalum capacitor.
24	LX1	Inductor Pins. Connect this pin to the switching node of inductor.
36	LX0	

PIN#	PIN Name	PIN Description
25	TG1	Top Gate Driver Outputs. Connect this pin to the gate of the top N-channel MOSFETs.
35	TG0	
26	BST1	Boot-strap Pins. Supply high side gate driver. Connect a 0.1μF ceramic capacitor between the BST and the LX pins.
34	BST0	
27	PGND1	Power Ground Pins. Connect this pin closely to the sources of the bottom N-channel MOSFETs, the (-) terminals of C_{VINT} and C_{VIN}.
33	PGND0	
28	BG1	Bottom Gate Driver Outputs. Connect this pin to the gate of the bottom N-channel MOSFETs.
32	BG0	
29	V_{EXT}	External Power Supply Pin. When V_{EXT} is higher than 4.7V, the V_{EXT} supplies the IC power, bypassing the internal LDO. Do not exceed 5.5V on this pin.
30	V_{INT}	Internal 5V LDO Output. The control circuits are biased from this voltage. Decouple this pin to PGND with a minimum of 4.7μF low ESR ceramic or tantalum capacitor.
31	V_{IN}	Main Input Supply. Decouple this pin to PGND with a capacitor.
37	PG1	Power Good Indictors. The open drain output is pulled high by external resistor when the output voltage is within 90% to 110% of regulation point.
38	PG0	
39	FAULTB1	Fault Indictors. The open drain output is pulled low during fault conditions.
40	FAULTB0	
41	SYNC	Switching Frequency Synchronization Pin. It can be programmed as SYNC Input or SYNC Output by the SYNC_CFG pin.
42	PHASE	Phase Programmable Pin. This pin determines the relative phases between the internal controllers and the phasing of the SYNC signal when the SYNC pin is programmed as SYNC Input.
43	RT	Frequency Set Pin. Tie high/low or a resistor between this pin and AGND sets the switching frequency. This pin sources 20μA.
44	SYNC_CFG	SYNC Configuration Pin. When the SYNC_CFG pin is floating or tied to V_{DD33}, the SYNC pin is programmed as SYNC Input; When the SYNC_CFG pin is tied to AGND, the SYNC pin is programmed as SYNC Output.
45	T_{SNS1}	External Temperature Sense Pins. Connect through a PNP transistor and a bypass capacitor to AGND in order to sense remote temperature. If external temperature sensing is not enabled, short the pin to ground through a 1kΩ resistor.
46	T_{SNS0}	

ORDER INFORMATION

PART NUMBER	FINISH	MARKING	PACKAGE TYPE	PACKING MATERIAL	MSL	TEMPERATURE RANGE
ES5201IUJ#PBF	Sn(RoHS)	5201	QFN	TRAY	1	-40°C to 125°C
ES5201IUJ#TRPBF	Sn(RoHS)	5201	QFN	TAPE&REEL	1	-40°C to 125°C

ABSOLUTE MAXIMUM RATINGS

	MIN	TYP	MAX	UNIT
Terminal Voltage				
Supply Input Voltage V_{IN}	-0.3		42	V
Top Driver Supply Voltage BST0, BST1	-0.3		V_{IN}+6V	V
Switch Node Voltage LX0, LX1	-5		V_{IN}	V
V_{INT}, V_{EXT}, EN0, EN1, PG0, PG1, SCL, SDA, (BST0-LX0), (BST1-LX1)	-0.3		6	V
ALERTB, FAULTB0, FAULTB1, V_{OSP0}, V_{OSP1}	-0.3		6	V
CSP0, CSP1, CSN0, CSN1	-0.3		6	V
SS0, SS1, FB0, FB1, V_{OSN0}, V_{OSN1}, COMP0, COMP1, ILMT	-0.3		V_{INT}	V
SYNC_CFG, SYNC, PHASE, RT, ADDR0, ADDR1	-0.3		V_{INT}	V
LSL, LSH, T_{SNS0}, T_{SNS1}, V_{DD33}	-0.3		V_{INT}	V
Temperatures				
Internal Operating Temperature Range	-40		150	°C
Storage Temperature Range	-65		150	°C
Peak Solder Reflow Package Body Temperature		260		°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

ESD RATINGS

	VALUE	UNIT
HBM (Human Body Model)	2	kV
CDM (Charged Device Model)	2	kV

Note: JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process. JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

RECOMMENDED OPERATING CONDITIONS

	MIN	TYP	MAX	UNIT
Supply Input Voltage	4.5		40	V
Output Voltage	0.5		5.5	V
V_{EXT} Bias External Voltage	4.5		5.5	V
Junction Temperature Range	-40		125	°C

Note 1: The device is not guaranteed to function outside its operating conditions.
Note 2: The ES5201 includes over temperature protection. The over temperature protection is active when the die temperature reaches 160°C. Continuous operation above the recommended maximum operation junction temperature may impair device reliability.

ELECTRICAL CHARACTERISTICS

The Y denotes the specifications which apply T_A = -40°C to +125°C Full Temperature Range **(FTR)**(Note1). Typical values are at T_J = 25°C. V_{IN} = 12V, $V_{EN0,1}$ = 5V unless otherwise specified. The values are guaranteed by test, design or statistical correlation.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	FTR
MAIN CONTROL LOOP							
Input Voltage Range	V_{IN}		4.5		42	V	
Output Voltage Range	V_{OUT}		0.5		5.5	V	
Regulated V_{OUT} Feedback Voltage	$V_{FB0,1}$	COMP1,2 = 1.2V, (Note 2) -40°C < T_J < 125°C	496	500	504	mV	Y
Feedback Current	$I_{FB0,1}$	(Note 2)		-10	-60	nA	
Reference Voltage Line Regulation	$V_{REFLNREG}$	V_{IN} = 4.5V to 42V, (Note 2)		0.002	0.005	%/V	
Output Voltage Load Regulation	$V_{LOADREG}$	Measured in Servo Loop, (Note 2)					
		ΔCOMP Voltage = 1.2V to 0.7V		0.01	0.1	%	Y
		ΔCOMP Voltage = 1.2V to 1.7V		-0.01	-0.1	%	Y
Transconductance Amplifier g_m	g_m	(Note 2); COMP = 1.2V, Sink/ Source 5μA		2.0		mmho	
Feedback Overvoltage Lockout	V_{OVLK}	Measured at FB0,1	0.53	0.55	0.57	V	Y
V_{OSP} Input Impedance	R_{VOSP}	$V_{EN0,1}$ = 5V		96		kΩ	
Initialization Time	t_{INIT}	Time from V_{INT} Passes Rising Threshold until Soft Starts		0.25		ms	
Quiescent Current	I_Q	$V_{EN0,1}$ = 0V		3		mA	
		$V_{EN0,1}$ = 5V, No Switching		6		mA	
EN0,1 Rising Threshold	$V_{EN0,1\_R}$		1.18	1.22	1.26	V	Y
EN0,1 Threshold Hysteresis	$V_{EN0,1\ HYS}$			60		mV	
SS Charge Current	$I_{SS0,1}$	$V_{SS0,1}$ = 0V	0.8	1	1.2	μA	Y
CSP0,1 Pin Current	$I_{CSP0,1}$			±0.1	±0.3	μA	Y
CSN0,1 Pin Current	$I_{CSN0,1}$	$V_{CSN0,1}$ < V_{VINT} - 0.2V		±0.1	±0.3	μA	Y
		$V_{CSN0,1}$ ⩾ V_{VINT} - 0.2V		0.5	0.9	mA	Y
Maximum Current Sense Voltage	V_{CSMAX}	V_{CSN} = 1.2V, ILMT = 0V	55	60	65	mV	Y
		V_{CSN} = 1.2V, ILMT = 1/4 V_{VDD33}	44	48	52	mV	Y
		V_{CSN} = 1.2V, ILMT = FLOAT or 1/2 V_{VDD33}	32.5	36	39.5	mV	Y
		V_{CSN} = 1.2V, ILMT = 3/4 V_{VDD33}	8.5	12	15.5	mV	Y
		V_{CSN} = 1.2V, ILMT = V_{VDD33}	20.5	24	27.5	mV	Y
ILMT Input Impedance	R_{ILMT}			250		kΩ	
Current DAC Accuracy	$I_{DAC0,1}$	VOUT_COMMAND = 0x007F	62.5	63.5	64.5	μA	Y
		VOUT_COMMAND = 0x0080	-65	-64	-63	μA	Y
Current DAC LSB				0.5		μA	
LDOs AND V_{EXT}							

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	FTR
V_{INT} Regulator Output Voltage	V_{INT}	I_{VINT} = 0mA		5.0		V	
V_{INT} Load Regulation	V_{INT_REG}	I_{VINT} = 20mA		0.5	2	%	
V_{INT} UVLO Rising Threshold	$V_{VINT, UVLOR}$		3.9	4.1	4.3	V	
V_{INT} UVLO Falling Threshold	$V_{VINT, UVLOF}$			3.8		V	
V_{INT} Regulator Current Limit	I_{LDOLMT}			170		mA	
V_{EXT} Switchover Voltage	V_{VEXT}	V_{EXT} Ramping Up	4.5	4.7		V	
V_{EXT} Switchover Hysteresis	$V_{VEXTHYS}$			0.2		V	
V_{EXT} Voltage Drop	V_{VEXTD}	I_{VINT} = 20mA		60	100	mV	
V_{DD33} Regulator Output Voltage	V_{DD33}		3.2	3.3	3.4	V	
V_{DD33} UVLO Rising Threshold	$V_{VDD33, UVR}$			3.1		V	
V_{DD33} UVLO Falling Threshold	$V_{VDD33, UVF}$			3.0		V	
V_{DD33} Regulator Current Limit	$I_{LDO33LMT}$			70		mA	
POWER GOOD and FAULT							
Power Good Threshold	V_{PG}	FB0,1 with Respect to Set Output Voltage FB0,1 Ramping Down FB0,1 Ramping Up		 -10 10		 % %	
PG Pin Leakage Current	$I_{PG0, 1}$	$V_{PG0, 1}$ = 5V			±2	µA	Y
Power Good Delay	$t_{PG0,1R}$ $t_{PG0,1F}$	Low to High High to Low		1 60		µs µs	
Power Bad Pull Down Resistance	R_{PBAD}			75	200	Ω	
FAULTB Pin Leakage Current	$I_{FAULTB0, 1}$	$V_{FAULTB0, 1}$ = 5V			±2	µA	Y
FAULTB Pull Down Resistance				75	200	Ω	
SWITCHING FREQUENCY AND PLL							
RT Pin Output Current	I_{RT}	V_{RT} = 1V	19	20	21	µA	Y
High Fixed Frequency	F_S	V_{RT} = V_{INT} or FLOAT	570	600	630	kHz	
Low Fixed Frequency		V_{RT} = 0V	380	400	420	kHz	
Programmable Switching Frequency		R_{RT} = 30.1kΩ		300		kHz	
		R_{RT} = 68.1kΩ		800		kHz	
		R_{RT} = 84.5kΩ		1.0		MHz	
		R_{RT} = 102kΩ		1.2		MHz	
Synchronizable Frequency Range		SYNC Pin = External Clock	200		1300	kHz	
SYNC to CH0 Phase, SYNC OUT		SYNC_CFG Pin = 0V		0		Deg	
CH0 to SYNC Phase Relationship, SYNC Input		Phase Pin = 0V		60		Deg	
		Phase Pin = FLOAT		90		Deg	
		Phase Pin = V_{INT}		120		Deg	

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	FTR
SYNC High Voltage		SYNC_CFG Pin = 0V, V_{INT} = 5V	4.5	5		V	
SYNC Low Voltage		SYNC_CFG Pin = 0V			0.2	V	
SYNC Pin High Level		SYNC_CFG Pin = 5V	2.2			V	
SYNC Pin Low Level		SYNC_CFG Pin = 5V			0.5	V	
DRIVER							
TG/BG On-Resistance		Pull-Up		1		Ω	
		Pull-Down		1		Ω	
BST UVLO Rising Threshold	$V_{BST, UVLOR}$	With Respect to LX		2.4		V	
BST UVLO Falling Threshold	$V_{BST, UVLOF}$	With Respect to LX		2.1		V	
TG/BG Transition Time Rise Time Fall Time	 t_R t_F	 C_{LOAD} = 3.3nF C_{LOAD} = 3.3nF		 14 8		 ns ns	
TG off to BG On Delay		C_{LOAD} = 3.3nF		15		ns	
BG off to TG On Delay		C_{LOAD} = 3.3nF		15		ns	
TG Minimum On-Time	$t_{ON(MIN)}$			60		ns	
ADC READBACK							
V_{IN} Readback LSB	V_{INLSB}			8		mV	
V_{IN} Readback Range	V_{INRG}		0		42	V	
V_{IN} Readback Accuracy	V_{INACC}	V_{IN} < 20V	-2		+2	%	Y
V_{OUT} Readback LSB	V_{OUTLSB}			1		mV	
V_{OUT} Readback Range	V_{OUTRG}		0		5.5	V	
V_{OUT} Readback Accuracy	V_{OUTACC}		-2		+2	%	Y
Output Current Readback LSB	I_{OUTLSB}			15.6		µV	
Output Current Readback Range	I_{OUTRG}	Measured between (CSP - CSN) Pins	-116		116	mV	
Output Current Readback Accuracy	I_{OUTACC}	I_{OUT} > 2A	-2		+2	%	Y
External Temperature Readback LSB	T_{EXTLSB}			1		°C	
External Temperature Readback Accuracy			-3		+3	°C	
Internal Temperature Readback LSB	T_{INTLSB}			1		°C	
Internal Temperature Readback Accuracy			-2		+2	°C	
PMBus DC Characteristics							
SCL, SDA Logic High Voltage	$V_{IH, PMBUS}$		1.4			V	
SCL, SDA Logic Low Voltage	$V_{IL, PMBUS}$				0.4	V	
Leakage Current SCL, SDA, ALERTB			-2		2	µA	

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	FTR
Input Capacitance SCL, SDA					10	pF	
SDA Pull Down Resistance	R_{SDA}			55	150	Ω	
ALERTB Pull Down Resistance	R_{ALERTB}			75	200	Ω	
PMBus Timing Characteristics							
PMBus Operating Frequency	f_{SCL}		10		1000	kHz	
Bus Free Time	t_{BFT}	Between Stop and Start Condition	1.3			µs	
Hold Time	t_{HT}		0.6			µs	
Repeated Start Condition Setup Time	t_{RS}		0.6			µs	
Stop Condition Setup Time	t_{SC}		0.6			µs	
Data Hold Time	t_{DH}		0.3			µs	
Data Setup Time	t_{DS}		0.1			µs	
Clock Low Period	t_{LOW}		1.3			µs	
Clock High Period	t_{HIGH}		0.6			µs	

Note 1: The ES5201 is tested under pulsed load conditions such that $T_J \approx T_A$. The ES5201 is guaranteed over the full −40°C to 125°C internal operating temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

Note 2: The ES5201 is tested in feedback loop and measure the differential voltage between the FB and V_{OSN} pins.

REVISION HISTORY

REV.	DATE	CHANGES
D	Mar 2026	1. Page 32 Typical Application Update. 2. Page 35 TAPE&REEL Drawing Update.
C	Jan 2024	Page 25 Status_Word Behavior Update.
B	Oct 2023	1. Page 5 Order Infomation Update. 2. Page 33-35 Package Drawings Update.
A	Aug 2023	Initial Release

BLOCK DIAGRAM (ONLY ONE CHANNEL IS SHOWN)

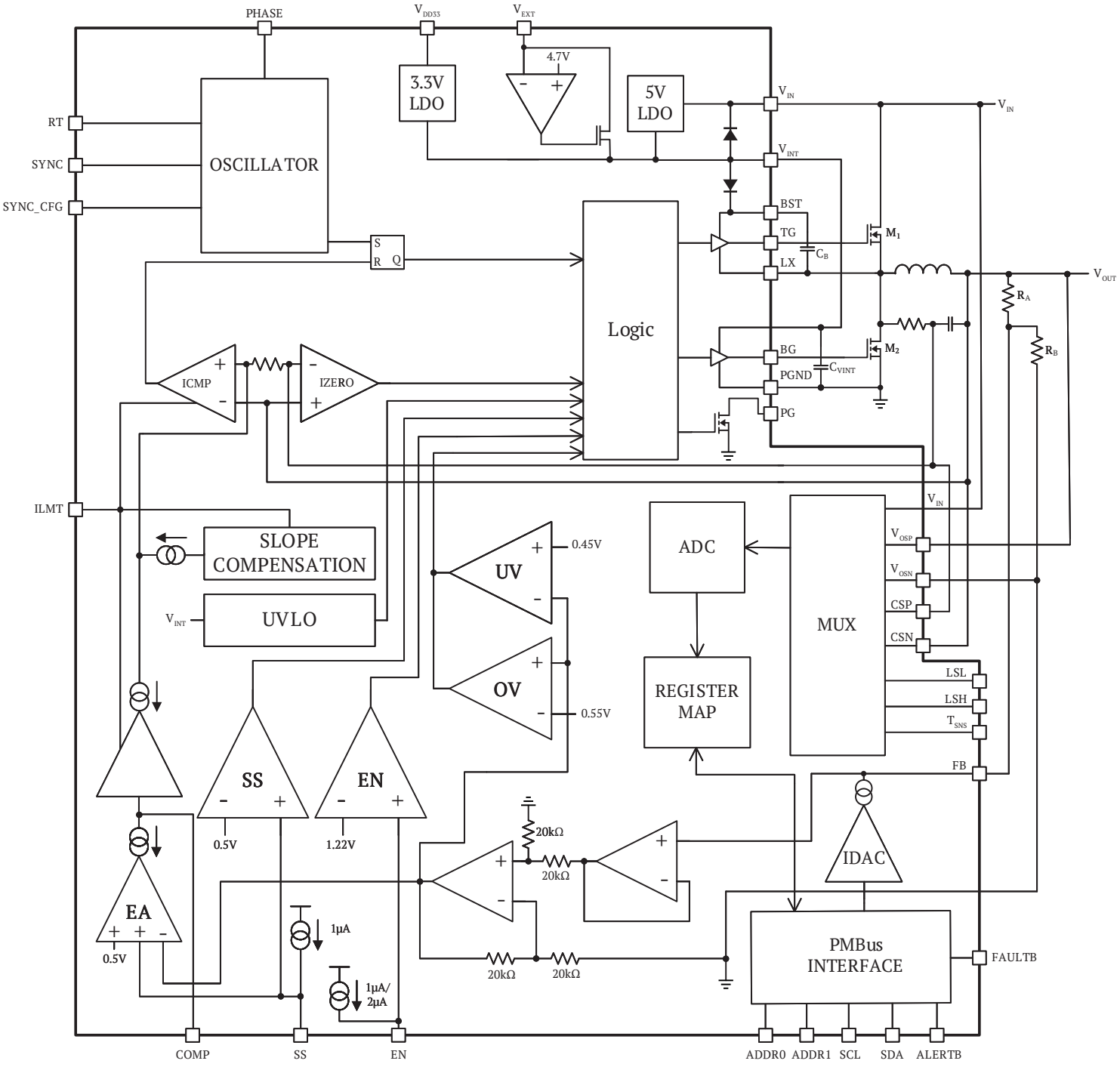
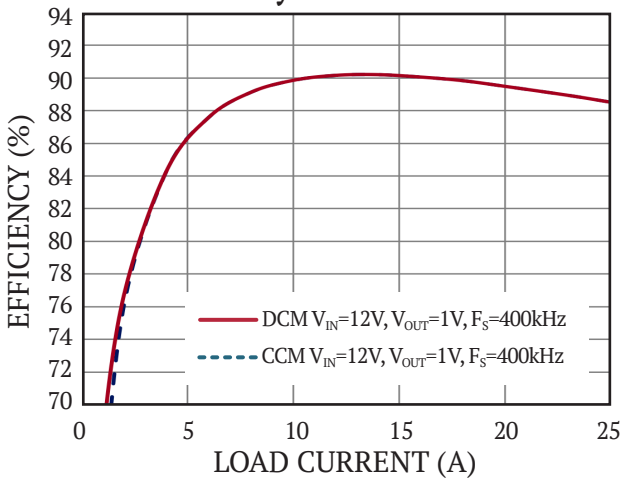


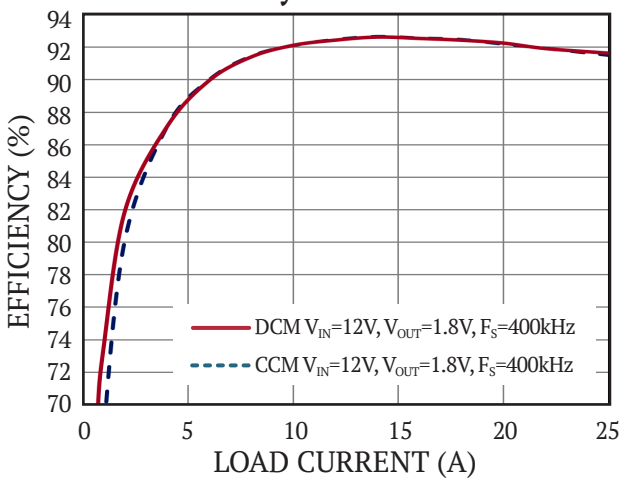
Figure 1 Simplified ES5201 Internal Function Block Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

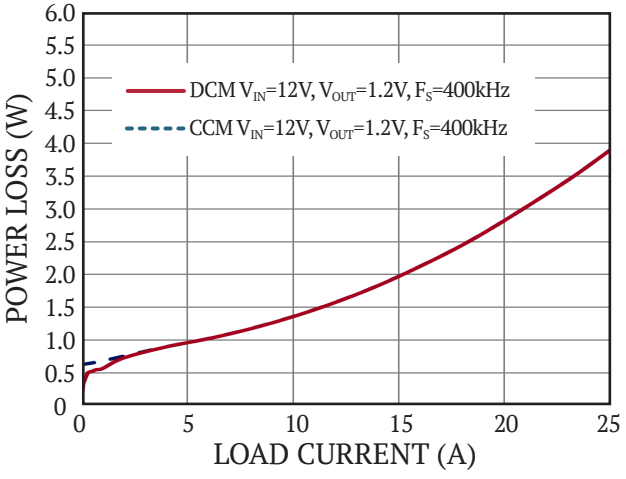
Efficiency vs Load Current



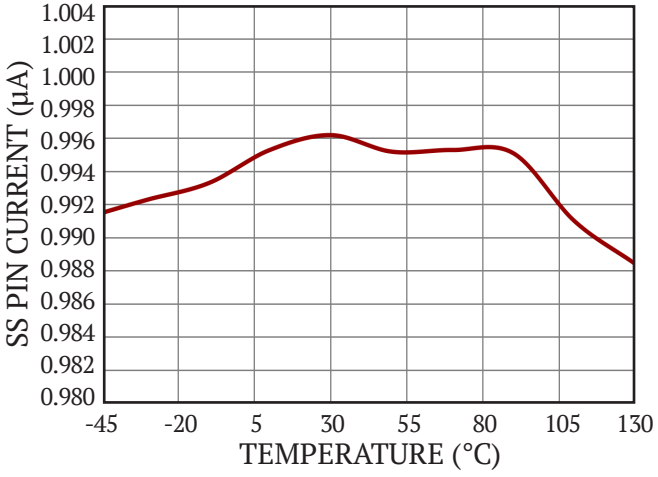
Efficiency vs Load Current



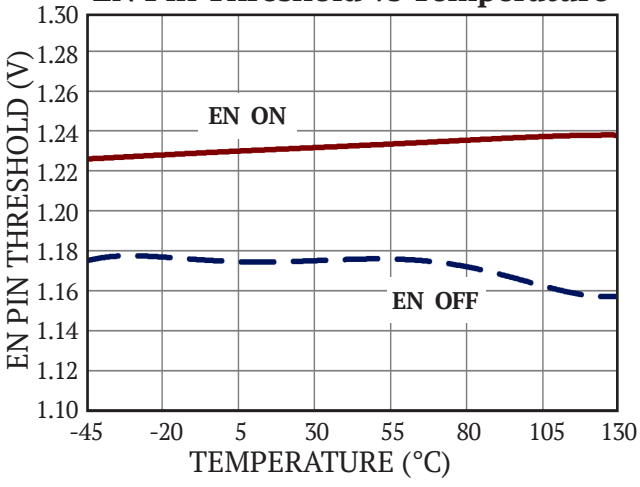
Power Loss vs Load Current



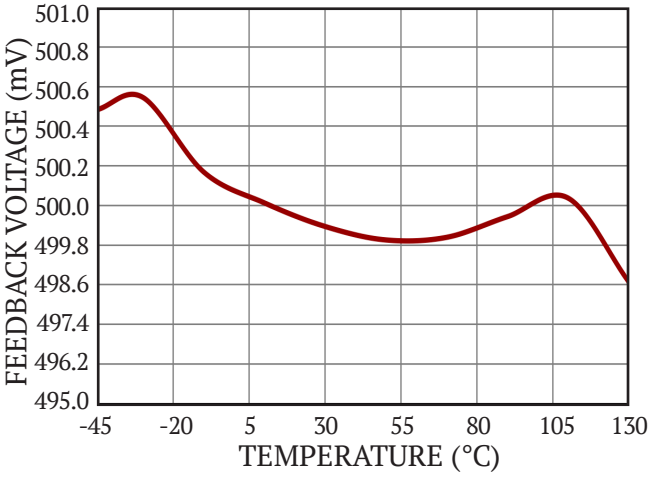
SS Pin Pull-Up Current vs Temperature



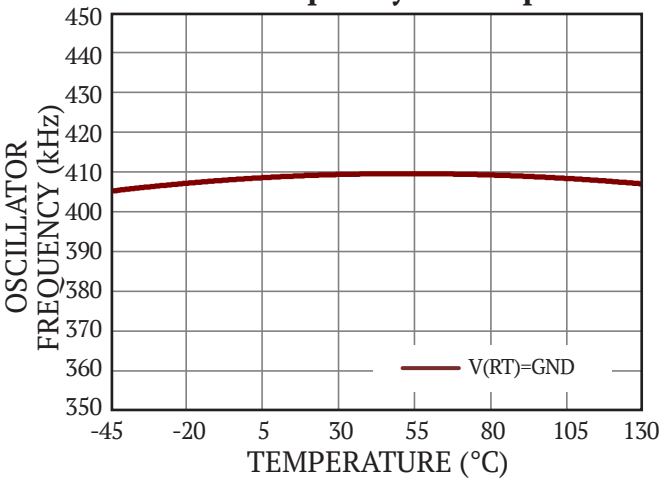
EN Pin Threshold vs Temperature



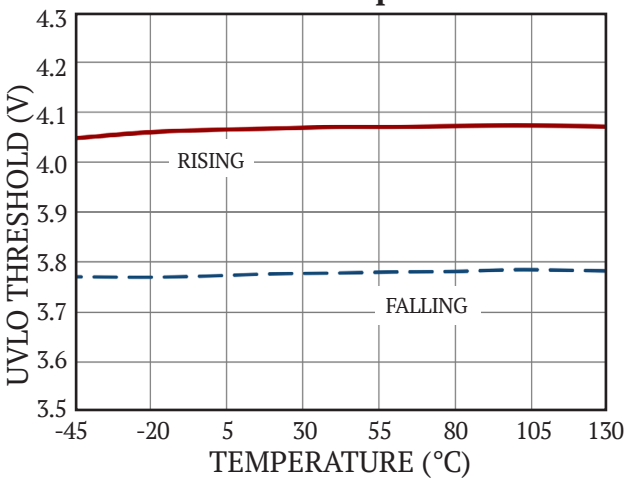
Regulated Feedback Voltage vs Temperature



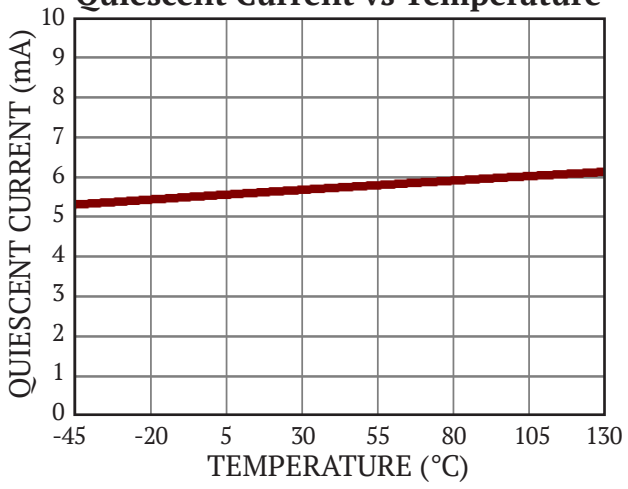
Oscillator Frequency vs Temperature



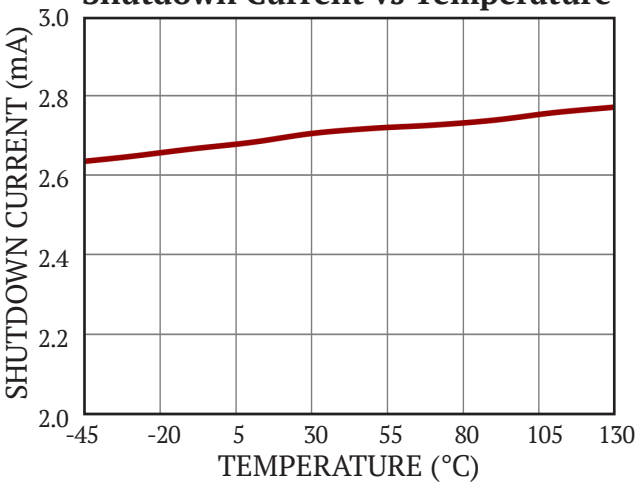
UVLO vs Temperature



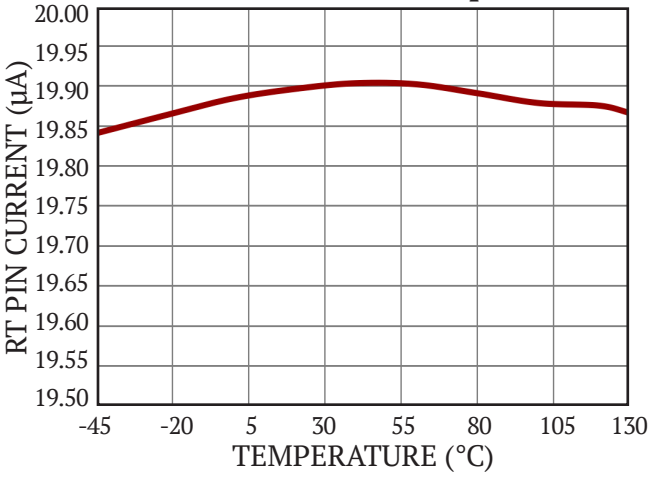
Quiescent Current vs Temperature



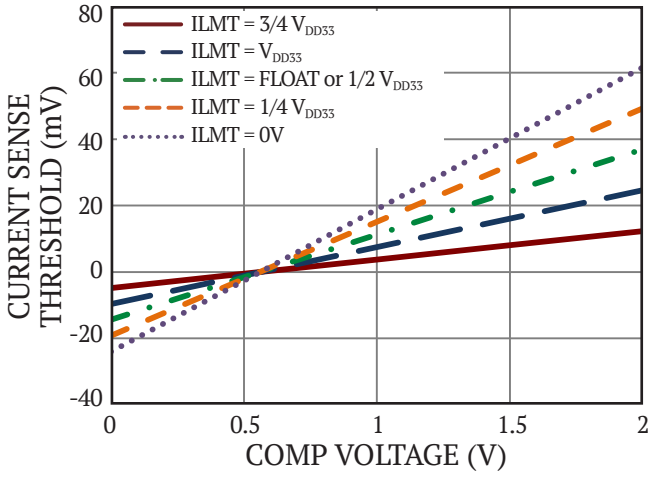
Shutdown Current vs Temperature



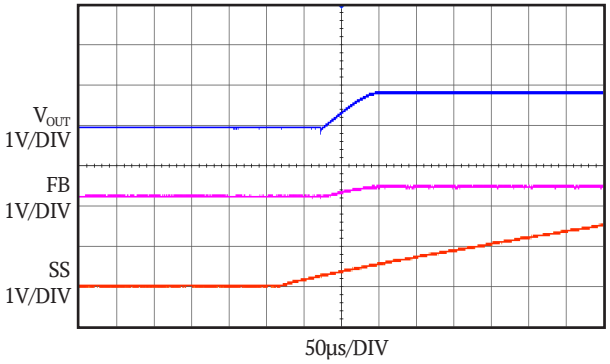
RT Pin Current vs Temperature



Current Sense Threshold vs COMP Pin Voltage

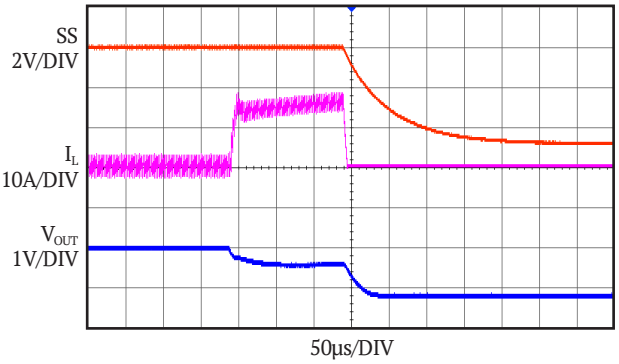


Start-up into a Prebiased Output



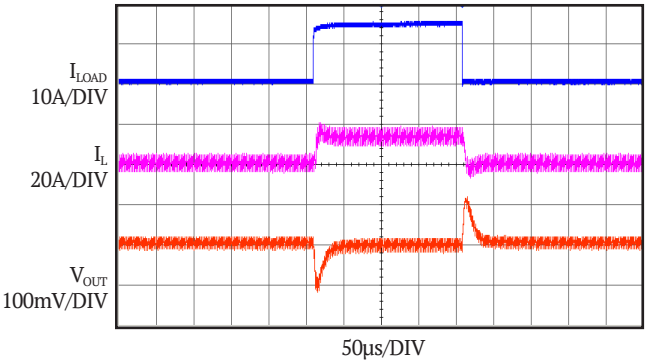
V_{IN}=12V,
V_{OUT}=1.2V

64-Cycle Overcurrent Counter to Hiccup



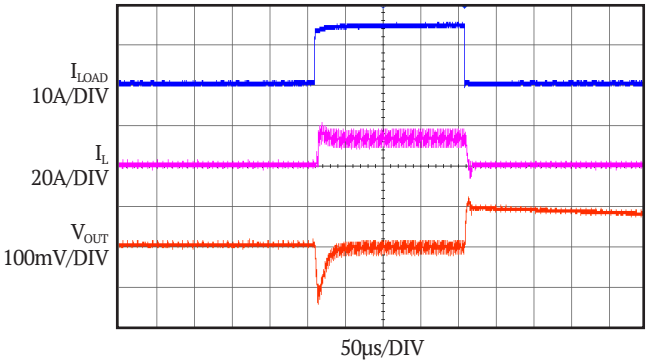
V_{IN}=12V,
V_{OUT}=1.2V

Load Step (CCM)



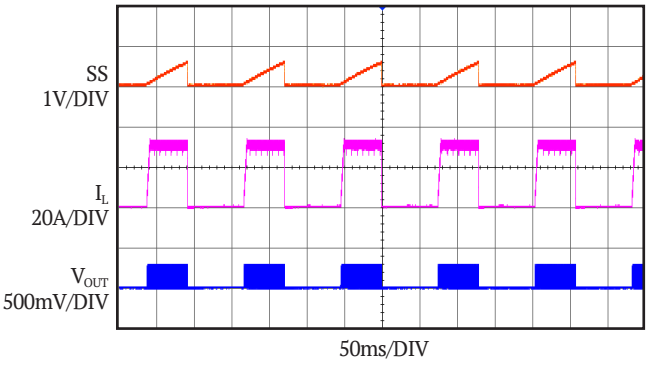
F_S=400kHz
V_{IN}=12V
V_{OUT}=1.8V

Load Step (DCM)

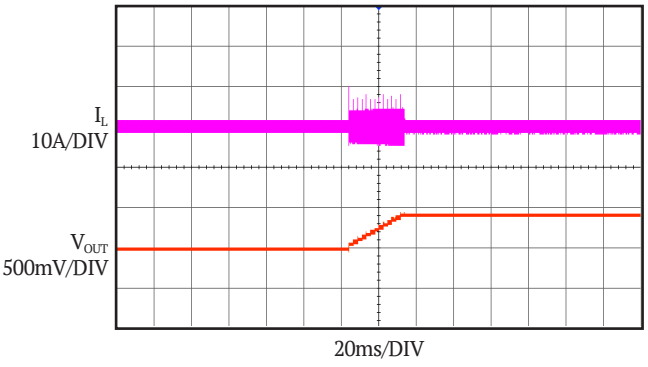


F_S=400kHz
V_{IN}=12V
V_{OUT}=1.8V

Start-up into Output Short

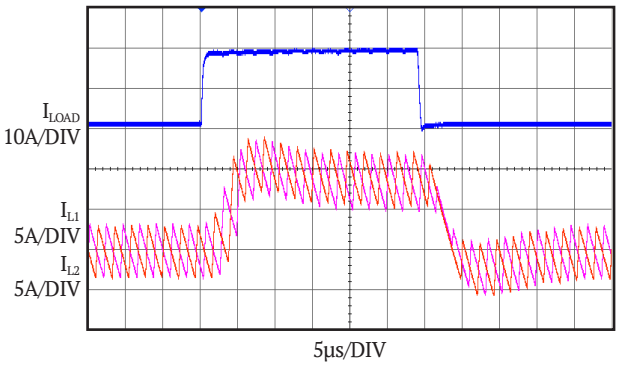


Output Program via PMBus Interface



F_S=400kHz
V_{IN}=12V
V_{OUT}=1.8V

2-Phase Dynamic Current Sharing



F_S =400kHz
V_{IN} = 12V
V_{OUT} = 1.8V

DETAILED DESCRIPTION

GENERAL FEATURES

The ES5201 is a high efficiency synchronous buck controller with PMBus compliant serial interface. It operates over a wide input range from 4.5V to 42V. It uses peak current mode control architecture for easy loop compensation, excellent line and load regulation, and flexible phase extension. The maximum current sense voltage is programmable from 12mV to 60mV with 12mV per step.

The two channels independently control their outputs up to 5.5V and always maintain 180° phase shift between the LX outputs. These two outputs can be paralleled to deliver higher current.

The controller integrates high-side and low-side MOSFET drivers capable of sourcing 2A and sinking 3A peak current. Adaptive dead-time control and driver's UVLO allow system optimization for high efficiency and reliability.

ENABLE CONTROL

The ES5201 has two precision enable control inputs. When each channel's EN pin voltage is greater than 1.22V, that channel is enabled. If the EN pin is pulled below 1.16V, that channel is disabled.

The PMBus interface is still active when both EN pins are low which means users can program the device and readback the internal register's value.

CONTROL LOOP

The ES5201 uses the output voltage information and the inductor current information to regulate the output voltage. The output voltage is differentially sensed by the FB and V_{OSN} pins. The sensed signal is compared with internal 0.5V reference and the voltage difference is amplified by a transconductance amplifier to the COMP pin. The COMP pin indicates the target peak inductor current. If the output voltage decreases, the ES5201 increases the target inductor peak current to raise the output voltage; if the output rises, the ES5201 decreases the target peak inductor current to reduce the output voltage.

At the beginning of each clock cycle, the high-side power MOSFET is turned on. When the inductor current reaches the peak current value set by the COMP pin, the high-side power MOSFET is turned off; the low-side power MOSFET is turned on. The high-side power MOSFET is turned on again at the beginning of next clock cycle. The controller regulates the output voltage by repeating this operation.

V_{INT} LOW DROPOUT REGULATOR (LDO) AND V_{EXT}

The ES5201 integrates one high performance, low dropout linear 5V V_{INT} regulator, which powers most blocks. The input voltage V_{IN} can be high up to 42V. Connect a minimum 4.7μF low ESR ceramic capacitor from the output V_{INT} to GND.

When the V_{INT} voltage is lower than the UVLO falling threshold of 3.8V, the ES5201 stops switching. It resumes switching after the V_{INT} voltage is higher than 4.1V.

The ES5201 internal power dissipation can be minimized by connecting the V_{EXT} to a 5V output or external supply. When the V_{EXT} voltage is higher than 4.7V, the V_{EXT} is internally connected to V_{INT} and the LDO is disabled. When the V_{EXT} voltage is lower than 4.5V, the connection between the V_{EXT} and the V_{INT} stops. Short the V_{EXT} pin to GND if it is not used. Don't apply more than 6V to the V_{EXT} pin.

START-UP

The ES5201 incorporates an external SS pin to smoothly ramp up the output to the desired voltage when the device is enabled. During start-up, an internal 1μA current source begins charging up the soft-start capacitor connected to the SS pin. The voltage error amplifier reference voltage is clamped to the voltage on the SS pin when the SS pin voltage is less than 0.5V. Therefore, the output voltage rises from 0V to regulation. The SS pin can also be used for tracking.

The soft-start time can be calculated based on the function below:

$$t_{SS} = \frac{0.5V \cdot C_{SS}(\mu F)}{1\mu A}$$

When the soft-start time set by the external capacitor is less than 1ms, an internal soft-soft circuit of 1ms takes over the soft-start.

If the output is pre-biased to a certain voltage before start-up, the ES5201 disables the switching of both the high-side and low-side power MOSFETs until the voltage

on the SS pin exceeds the sensed voltage by the FB and V_{OSN} pins.

OPERATION MODE

By default, the ES5201 operates in Continuous Conduction Mode (CCM). In CCM, low-side power MOSFET resumes switching neglecting zero load current condition.

If one channel's DCM bit in the MFR_SETTNG command is set to be 1, the channel operates in Discontinuous Conduction Mode (DCM). In DCM, the low-side power MOSFET turns off when the load current ramps to near zero, preventing recirculation current that can seriously reduce efficiency under light load condition.

When the SS pin is below 0.15V, the ES5201 always operates in DCM.

SWITCHING FREQUENCY SELECTION

The switching frequency of the ES5201 can be programmed in three methods: linearly program the frequency using an external resistor, simply selecting two fixed frequencies, synchronizing to an external clock as shown in Table 2.

Put a resistor between RT and AGND to linearly program the switching frequency as shown in Figure 2. The relationship can be approximately calculated by the function below:

$$F_S = 13.5 \cdot R_{RT} - 102kHz$$

where 20 kΩ ⩽ R_{RT} ⩽ 100 kΩ

To ease the external component design, the ES5201 can select two fixed frequencies with the RT pin. If the RT pin is connected to V_{INT} or floating, the switching frequency is set to 600kHz; if the RT pin is pulled to GND, the switching frequency is set to 400kHz.

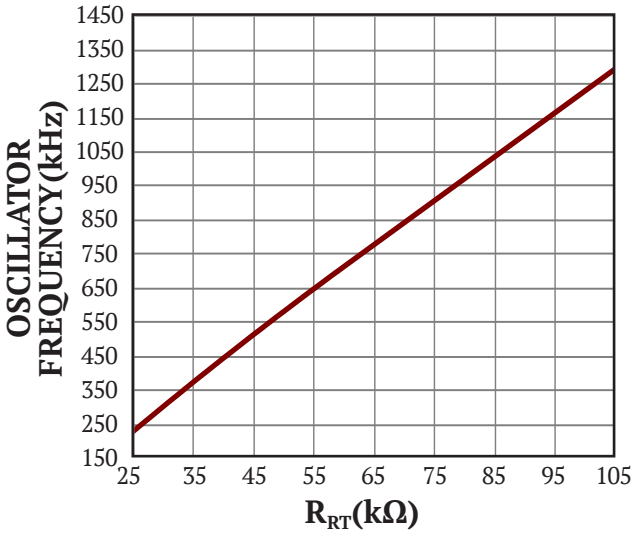


Figure 2 Relationship between Switching Frequency and RT Pin Resistor

When an external clock is applied to the SYNC pin and the SYNC pin is programmed as SYNC Input, the ES5201 switching frequency will automatically synchronize to the external clock. The relative phase between the external clock and channel 0 is programmed by the PHASE pin.

The ES5201 features a SYNC Input and Output function which allows multiple ES5201s to be daisy chained together in multiphase application. When the SYNC pin is programmed as SYNC Output, the channel 0 switching will be in the same phase with the SYNC pin.

Table 2 Frequency Setting

RT PIN	SYNC PIN	FREQUENCY
0V	0V or V_{INT}	400kHz
V_{INT} or FLOAT	0V or V_{INT}	600kHz
Resistor to AGND	0V or V_{INT}	200kHz to 1.2MHz
Any of Above	External Clock	SYNC to External Clock

DIFFERENTIAL OUTPUT VOLTAGE REMOTE SENSING

The ES5201 supports differential remote output voltage sense function. The dedicated V_{OSN} pin helps provide the remote GND voltage sense, cooperating with remote output feedback voltage sense pin FB. Differential output voltage remote sensing allows for more accurate output regulation in high power distributed systems which have large line losses.

OUTPUT VOLTAGE SETTING AND PROGRAMMING

The ES5201 output voltage is set by the two resistors between the V_{OUT}, FB, and V_{OSN} pin as shown in Figure 3. The output voltage can be calculated by the function:

$$V_{OUT} = 0.5V \cdot (1+\frac{R_A}{R_B}) - I_{DAC\_Total} \cdot R_A$$

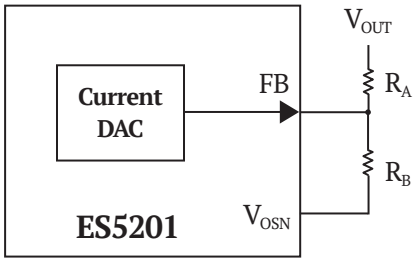


Figure 3 V_{OUT} Setting and Programming

where IDAC can be programmed by the PMBus. The programmable range is -64μA ⩽ IDAC ⩽ 63.5μA. By default, the IDAC output is 0μA.

POWER GOOD INDICATOR

The PG pin is an open drain power good indicator controlled by a windows comparator. If the regulated feedback voltage (FB-V_{OSN}) is within the ±10% window of 500mV reference voltage, the PG pin will be high impedance. The PG pin should be connected to V_{INT} or another voltage source through a typical 10kΩ ~ 100kΩ resistor.

When the regulated feedback voltage leaves the ±10% window of 500mV reference voltage, the PG pin will be pulled low after a 60μs deglitch filter.

CURRENT LIMIT SETTING

The ILMT pin is a 5-level logic input which sets the maximum current sense voltage of the controller. Table 3 shows the ILMT setting. These settings represent the maximum inductor current setting. The average inductor current is lower than the peak current due to the ripple current. As a result, the current limit setting should be higher than the average inductor current with enough design margin. There is a 500k pull down resistor from the ILMT pin to AGND and a 500k pull up resistor from ILMT pin to V_{DD33}.

Table 3 ILMT Setting

ILMT Pin Voltage	Maximum Current Sense Voltage
0V	60mV
1/4 V_{VDD33}	48mV
1/2 V_{VDD33} or FLOAT	36mV
3/4 V_{VDD33}	12mV
V_{VDD33}	24mV

EXTERNAL TEMPERATURE MONITOR

The ES5201 features external temperature sensing for each channel with the T_{SNS0} and T_{SNS1} pins. Each T_{SNS} pin is connected to quiet analog ground using a diode-connected PNP transistor such as MMBT3906 as shown in Figure 4. The voltage on the TSNS pin is digitized by the ADC and the computed external sensed temperature is returned by the paged READ_TEMPERATURE_1 command.

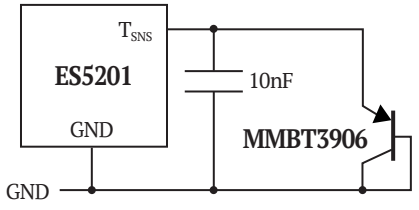


Figure 4 External Temperature Sense

OVER VOLTAGE PROTECTION

The ES5201 features output over voltage protection. If the sensed feedback voltage is higher than 550mV, the low-side Power MOSFET will keep on until the sensed feedback voltage drops back to the ±10% window of 500mV reference voltage.

OVER CURRENT PROTECTION (HICCUP MODE)

The ES5201 continuously monitors the inductor current. When an overcurrent fault is detected for 64 consecutive clock cycles, the controller turns off both the high-side and low side power MOSFET, resets the soft-start capacitor and waits for 32768 clock cycles before attempting to start-up again.

OVER TEMPERATURE PROTECTION

When the ES5201 die temperature reaches 160°C, the switching stops and both SS pins are pulled to ground. The ES5201 goes back switching after the die temperature reduces to be less than 140°C.

MINIMUM ON-TIME

The minimum on-time, $t_{ON(MIN)}$, is the smallest time that the ES5201 is capable of turning on the top Power MOSFET. It is determined by the gate charge and the internal timing delays. The minimum on-time design should meet the following equation:

$$t_{ON(MIN)} < \frac{V_{OUT}}{V_{IN} \cdot F_S}$$

The minimum on-time of the ES5201 is 60ns. If the system design cannot meet the minimum on-time requirement, it will skip pulse.

TRANSIENT IMPROVEMENT OPERATION

ES5201 features a proprietary transient improvement function. When the ENFAST Bit in MFR_SETTING command is set, the load transient improvement feature is enabled. During a large step-down load transient, the ES5201 will increase the switching frequency for several clock cycles to reduce the output voltage drop. This feature can only be enabled for single output applications.

MULTI-PHASE OPERATION

The ES5201 can be configured for single output multi-phase operation by making these connections:

Tie the EN, COMP, SS, FB, SYNC pins of parallel channels together. Program one ES5201 as SYNC Output and all other ES5201s as SYNC Input or program all ES5201 as SYNC Input and apply external clock on the SYNC pins.

PMBUS INTERFACE

PMBus is a two-wire serial interface which is used for communication between ICs and systems. The bus consists of a clock line (SCL) and a data line (SDA). A PMBus master controls the bus by generating the SCL signal and controlling the data transfer. The ES5201 works as PMBus slave to support the data transfer. It can operate at any frequency up to 1MHz.

PMBUS TRANSFER FORMAT

The Figure 5 shows the timing relationship of the signal of the bus.

The PMBus master transmits a START condition to begin the communication. The START signal is generated by transitioning SDA from high to low while keeping SCL high. Once the data transfer finishes, the master transmits a STOP signal to end the communication. The STOP signal is transmitted by master by pulling SDA from low to high while the SCL is high. The PMBus Write and Read command format is shown in Figure 5.

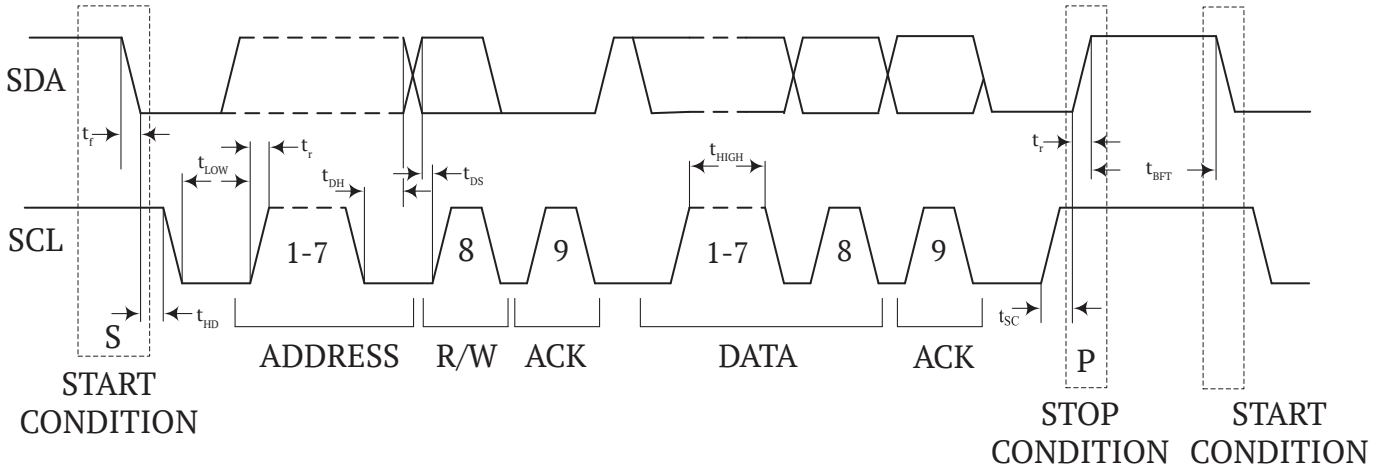
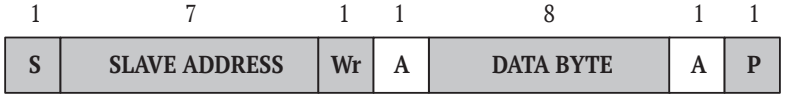
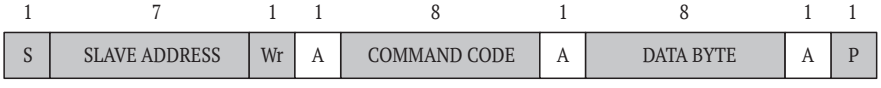


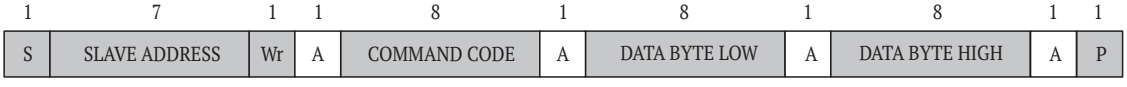
Figure 5 PMBus Timing Diagram



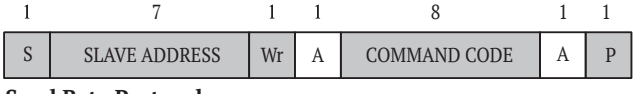
S Start Condition
Sr Repeated Start Condition
Rd Read(BIT VALUE = 1)
Wr Write(BIT VALUE =0)
A Acknowledge(This BIT = 0 for an ACK or 1 for a NACK)
P Stop Condition
Slave to Master
Master to Slave



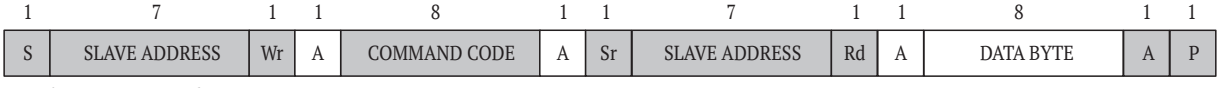
Write Byte Protocol



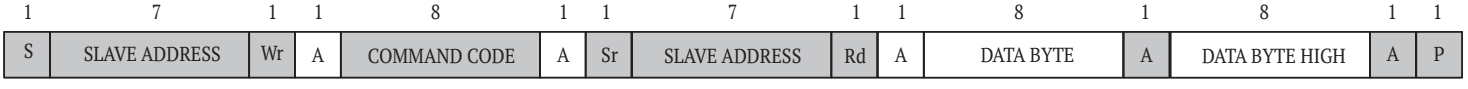
Write Byte Protocol



Send Byte Protocol



Read Byte Protocol



Read Word Protocol

Figure 6 Write and Read Protocol

PMBUS ADDRESS

The ES5201 offers three different type PMBus addressing: global, device, and rail.

Global addressing allows the PMBus master to address all ES5201 devices on the bus. Global address cannot be disabled. There are two global address. One ES5201 global address is fixed 0x7A (7 bit). Commands sent to this global address act the same as Page is set to 0xFF. The other global address 0x7B (7 bit) is paged and allows channel specific command. Reading from global address is strongly discouraged.

Device addressing is the standard addressing method. In ES5201, the device address is set by the combination of the ADDR0 and ADDR1 pins as shown in Table 4. ADDR0 and ADDR1 individually connect through R_{TOP} and R_{BOT} between V_{DD33} and AGND pins. Device addressing is stored at MFR_ADDRESS register.

Table 4 PMBus Address Setting

R_{TOP} (kΩ)	R_{BOT} (kΩ)	ADDR1 Pin Device Address [6:4]	ADDR0 Pin Device Address [3:0]
Open	0	000	0000
37.4	2.67	001	0001
37.4	5.76	010	0010
37.4	9.31	011	0011
37.4	13.7	100	0100
37.4	18.7	101	0101
37.4	24.9	110	0110
28.7	24.9	111	0111
24.9	28.7	000	1000
24.9	37.4	001	1001
18.7	37.4	010	1010
13.7	37.4	011	1011
9.31	37.4	100	1100
5.76	37.4	101	1101
2.67	37.4	110	1110
0	Open	111	1111

Rail addressing allows the PMBus master to simultaneously communicate with all channels in multi-phase system. The rail address can be assigned with the paged MFR_RAIL_ADDRESS command. Reading from rail address is strongly discouraged.

PMBUS COMMAND DETAILS

Table 5 PMBus Command Summary

CMD CODE	COMMAND NAME	TYPE	PAGED	DEFAULT	UNITS	DESCRIPTION
00h	PAGE	R/W Byte	N	0x00		Provide support for multiple outputs.
01h	OPERATION	R/W Byte	Y	0x80		Turn the unit on and off in conjunction with the EN pin.
03h	CLEAR_FAULTS	Send Byte	Y			Clear any fault bits that have been set.
20h	VOUT_MODE	R Byte	Y	0x40		Output voltage format.
21h	VOUT_COMMAND	R/W Word	Y	0x0000		Adjust the output voltage.
24h	VOUT_MARGIN_HIGH	R/W Word	Y	0x0000		Adjust the output voltage.
25h	VOUT_MARGIN_LOW	R/W Word	Y	0x0000		Adjust the output voltage.
38h	IOUT_CAL_GAIN	R/W Word	Y		15.625 μΩ	The ratio of the voltage at the current sense pins to the current.
42h	VOUT_OV_WARN_LIMIT	R/W Word	Y	0x1388	1mV	Output overvoltage warning limit.
4Ah	IOUT_OC_WARN_LIMIT	R/W Word	Y	0x0600	62.5mA	Output overcurrent warning limit.

CMD CODE	COMMAND NAME	TYPE	PAGED	DEFAULT	UNITS	DESCRIPTION
51h	OT_WARN_LIMIT	R/W Word	Y	0x0091	1°C	Output overtemperature warning limit.
57h	VIN_OV_WARN_LIMIT	R/W Word	N	0x1480	8mV	Input overvoltage warning limit.
78h	STATUS_BYTE	R Byte	Y	0x00		One-byte summary of the unit's fault condition.
79h	STATUS_WORD	R Word	Y	0x0000		Two-byte summary of the unit's fault condition.
88h	READ_VIN	R Word	N	0x0000	8mV	Measured V_{IN} voltage.
8Bh	READ_VOUT	R Word	Y	0x0000	1mV	Measured V_{OUT} voltage.
8Ch	READ_IOUT	R Word	Y	0x0000	62.5mA	Measured output current.
8Dh	READ_TEMPERATURE_1	R Word	Y	0x0019	1°C	External sensed temperature.
8Eh	READ_TEMPERATURE_2	R Word	N	0x0019	1°C	Internal sensed temperature.
98h	PMBUS_REVISION	R Byte	N	0x33		PMBus revision supported by this device.
99h	MFR_DEVICE_ID	R Byte	N	0x80		Device ID.
9Ah	MFR_PIN_SETTING	R Byte	N			Device ILMT, RT, MODE Pins setting.
ABh	MFR_VOUT_PEAK	R Word	Y	0x0000	1mV	Maximum measured value of READ_VOUT.
B1h	MFR_IOUT_CAL_GAIN_TC	R/W Byte	N			Temperature coefficient of the current sensing element.
BBh	MFR_VIN_PEAK	R Word	N	0x0000	8mV	Maximum measured value of READ_VIN.
BCh	MFR_IOUT_PEAK	R Word	Y	0x0000	62.5mA	Maximum measured value of READ_IOUT.
BDh	MFR_TEMPERATURE_1_PEAK	R Word	Y	0x0019	1°C	Maximum measured value of READ_TEMPERATURE_1.
BEh	MFR_TEMPERATURE_2_PEAK	R Word	N	0x0019	1°C	Maximum measured value of READ_TEMPERATURE_2.
BFh	MFR_CLEAR_PEAKS	Send Byte	N			Clears all peak values.
C7h	MFR_VOUT_SLEW_RATE	R/W Byte	Y	0x00		Output voltage adjustment slew rate.
C9h	MFR_ADDRESS	R Byte	N			Record the PMBus address set by the ADDR pins.
CAh	MFR_RAIL_ADDRESS	R/W Byte	Y	0x00		Set the PMBus rail address.
CBh	MFR_SETTING	R/W Byte	N	0x00		Adjust ES5201 Setting (DCM, ENFAST).
CCh	MFR_SMBALERT_MASK	R/W Byte	N	0x00		Blank signal to trigger ALERTB pin.
CFh	MFR_RESET	Send Byte	N	0x00		Reset the PMBus.

PAGE (00h)

The PAGE command provides the ability to configure, control, and monitor ES5201 both channels through only one PMBus address. Each Page has its own operating commands. The data byte for the PAGE command is an unsigned binary integer.

In the ES5201, Pages 0x00 and 0x01 correspond to Channel 0 and Channel 1, respectively. Setting PAGE to 0xFF applies any paged commands to both channels. With PAGE set to 0xFF, the ES5201 will respond to read commands as if PAGE is set to 0x00 (Channel 0).

The default value for PAGE is 0x00.

OPERATION (01h)

The OPERATION command is used to turn the device output on or off in conjunction with the input from the EN pins. It is also used to set the output voltage to upper or low margin voltages.

OPERATION is a paged command. In order to access OPERATION command for channel 0 of the ES5201, PAGE must be set to 0x00. In order to access OPERATION command for channel 1 of the ES5201, PAGE must be set to 0x01. For simultaneous access of both channels, PAGE command must be set to 0xFF.

The ON bit (BIT[7]) has the same function as the EN pin. The output is on when both the ON bit and the EN pin are high. The ON bit is automatically reset to 1 after an EN pin shutdown, power cycle, or MFR_RESET command. The default value for OPERATION is 0x80. Writing an unsupported OPERATION value will generate a CML fault and the command will be ignored.

Table 6 OPERATION command Supported Value

Supported Command Value	MEANING
0x00	Immediate off
0x80	On
0xA8	Margin high
0x98	Margin low

CLEAR_FAULTS (03h)

The CLEAR_FAULTS command is used to clear any fault bits that have been set in the STATUS_BYTE and STATUS_WORD Registers. At the same time, the ES5201 releases its ALERTB pin if it is asserted. If the fault is still present when the bit is cleared, the fault bit will remain set and the host notified by asserting the ALERTB pin low.

CLEAR_FAULTS is a paged command. This write-only command has no data bytes. Issuing a CLEAR_FAULTS command will not cause the device to restart in the event of a fault turn-off.

VOUT_MODE (20h)

The VOUT_MODE command reads and commands the output voltage. The 3 MSBs determine the data format (only direct format is supported in ES5201), and the other 5 bits represent the exponent used in the output voltage read/write commands. The default value of VOUT_MODE is 0x40. The VOUT_MODE is a Read Only command. If a host sends a VOUT_MODE write command, the ES5201 rejects the VOUT_MODE command, declare a communication fault (CML) for invalid data.

VOUT_COMMAND (21h)

Command						VOUT_COMMAND										
Format						Direct										
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Function	X					$R_A \cdot 0.5\mu A/LSB$										

The VOUT_COMMAND controls a current DAC value used to adjust the output. The current is injected to the FB pin. The 8 LSB byte is formatted as an 8-bit 2's complement value. Setting BIT[7] = 0 to reduce the output voltage and BIT[7] =1 to increase the output voltage. The details are listed below. The default value for this command is 0x0000. VOUT_COMMAND is a paged command.

BIT	VALUE	Function
7	0	0
	1	64μA · R_A
6	0	0
	1	-32μA · R_A
5	0	0
	1	-16μA · R_A
4	0	0
	1	-8μA · R_A
3	0	0
	1	-4μA · R_A
2	0	0
	1	-2μA · R_A
1	0	0
	1	-1μA · R_A
0	0	0
	1	-0.5 μA · R_A

VOUT_MARGIN_HIGH (24h)

The VOUT_MARGIN_HIGH has the same contents as the VOUT_COMMAND. When OPERATION=0xA8, the VOUT_MARGIN_HIGH command controls the output voltage instead of VOUT_COMMAND. The default value for this command is 0x0000. It is a paged command.

VOUT_MARGIN_LOW (25h)

The VOUT_MARGIN_LOW has the same contents as the VOUT_COMMAND. When OPERATION=0x98, the VOUT_MARGIN_LOW command controls the output voltage instead of VOUT_COMMAND. The default value for this command is 0x0000. It is a paged command.

IOUT_CAL_GAIN (38h)

The IOUT_CAL_GAIN is the ratio of the voltage at the current sense element to the sensed current. The effective current sense element is the DCR of the inductor. The resolution is 15.625μΩ. The range is 0.0625mΩ to 4mΩ. If a host sends a value less than 0.0625mΩ, the ES5201 rejects the command, declare a communication fault (CML) for invalid data.

The IOUT_CAL_GAIN is a paged command. The IOUT_CAL_GAIN default value is set by the LSL and LSH pins as shown in Table 7. If both LSL and LSH are shorted to ground, the IOUT_CAL_GAIN is set to be default 1mΩ.

Command						IOUT_CAL_GAIN									
Format						Direct									
Default						Set by LSH and LSL pins									
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Function	X					15.625 μΩ/LSB										

Table 7 IOUT_CAL_GAIN Setting

RTOP (kΩ)	RBOT (kΩ)	LSH Pin	LSL Pin
		IOUT_CAL_GAIN [7:4]	IOUT_CAL_GAIN [3:0]
Open	0	0000	0000
37.4	2.67	0001	0001
37.4	5.76	0010	0010
37.4	9.31	0011	0011
37.4	13.7	0100	0100
37.4	18.7	0101	0101
37.4	24.9	0110	0110
28.7	24.9	0111	0111
24.9	28.7	1000	1000
24.9	37.4	1001	1001
18.7	37.4	1010	1010
13.7	37.4	1011	1011
9.31	37.4	1100	1100
5.76	37.4	1101	1101
2.67	37.4	1110	1110
0	Open	1111	1111

Where RTOP is the resistor between LSH or LSL and VDD33; RBOT is the resistor between LSH or LSL and ground.

VOUT_OV_WARN_LIMIT (42h)

The VOUT_OV_WARN_LIMIT command sets the value of the output voltage measured by the ADC that causes an output overvoltage warning. The READ_VOUT value will be used to determine if this limit has been exceeded. If the sensed voltage exceeds this value, the VOUT bit is set in STATUS_WORD command, and the ALERTB signal is asserted. This command has two data bytes and is formatted as unsigned binary. The default value for this command is 0x1388 which is 6V.

Command						VOUT_OV_WARN_LIMIT									
Format						Unsigned binary									
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	1	0	0	1	1	1	0	0	0	1	0	0	0
Function	x		1mV/LSB													

IOUT_OC_WARN_LIMIT (4Ah)

The IOUT_OC_WARN_LIMIT command sets the value of the output current measured by the ADC that causes an output overcurrent warning. The READ_IOUT value will be used to determine if this limit has been exceeded. If the sensed current exceeds this value, the IOUT bit is set in STATUS_WORD command, and the ALERTB signal is asserted. This command has two data bytes and is formatted as unsigned binary. The default value for this command is 0x0600 which is 96A.

Command						IOUT_OC_WARN_LIMIT										
Format						Unsigned binary										
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0
Function	X		62.5mA/LSB													

OT_WARN_LIMIT (51h)

The OT_WARN_LIMIT command sets the threshold for external temperature measured by the TSNS pin. If the sensed temperature exceeds this value, the OT warning bit is set in STATUS_BYTE, and the ALERTB signal is asserted. The READ_TEMPERATURE_1 value is used to determine if the limit has been exceeded. This command has two data bytes and is formatted as unsigned binary. The default value for this command is 0x0091 which is 145°C.

Command						OT_WARN_LIMIT										
Format						Unsigned binary										
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	1
Function	X					1°C/LSB										

VIN_OV_WARN_LIMIT (57h)

The VIN_OV_WARN_LIMIT command sets the value of the input voltage measured by the ADC that causes an input overvoltage warning. The READ_VIN value will be used to determine if this limit has been exceeded. If the sensed voltage exceeds this value, the VIN Bit is set in STATUS_WORD, and the ALERTB signal is asserted. This command has two data bytes and is formatted as unsigned binary. The default value for this command is 0x1480 which is 42V.

Command						VIN_OV_WARN_LIMIT										
Format						Unsigned binary										
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	1	0	1	0	0	1	0	0	0	0	0	0	0
Function	x		8mV/LSB													

STATUS_BYTE (78h)

The STATUS_BYTE command returns one byte of information with a summary of the most critical faults. The STATUS_BYTE is a paged register.

BIT	BIT NAME	BEHAVIOR	DESCRIPTION
7	RESERVED		Always read as 0.
6	OFF	Live	This bit is set if the channel is off, regardless of the reason, including simply the EN pin is low.
5:3	RESERVED		Always read as 0.
2	OT	Live	A temperature fault or warning has occurred.
1	CML	Latched	A communication fault has occurred.
0	NONE_OF_THE_ABOVE	Live	Always read as 0.

STATUS_WORD (79h)

The STATUS_WORD command returns two-byte of information with a summary of the most critical channel's fault condition. The low byte of the STATUS_WORD is the same as the STATUS_BYTE command. The STATUS_WORD is a paged command.

BIT	BIT NAME	BEHAVIOR	DESCRIPTION
15	V_{OUT}	Latched	An output voltage fault or warning has occurred.
14	I_{OUT}	Latched	An output current fault or warning has occurred.
13	V_{IN}	Live	An input voltage fault or warning has occurred.
12	RESERVED		Always read as 0.
11	PGOODB	Live	The Power Good state is false if this bit is set.
10:8	RESERVED		Always read as 0.

READ_VIN (88h)

The READ_VIN command returns two bytes of data in the direct data format that represent the input voltage. It is formatted as a 14-bit unsigned binary integer scaled 8mV/ bit. READ_VIN is not a paged register. The READ_VIN is read only command and the default value is 0x0000.

Command	READ_VIN
Format	Direct
LSB	8mV
Default	0x0000

READ_VOUT (8Bh)

The READ_VOUT command returns two bytes of data in the direct data format that represent the output voltage measured between the VOSP and VOSN pins. It is for matted as a 14-bit unsigned binary integer scaled 1mV/ bit. READ_VOUT is a paged register. PAGE register cannot be set to 0x11 for READ_VOUT command. The READ_VOUT is read only command and the default value is 0x0000.

Command	READ_VOUT
Format	Direct
LSB	1mV
Default	0x0000

READ_IOUT (8Ch)

The READ_IOUT command returns the 14-bit measured value of the output current. The reading from the Measurement System must be manipulated in order to convert the measured value into the desired value (IOUT). READ_IOUT is a paged command.

Command						READ_IOUT									
Format						Direct, 2's complement									
Default						0x0000									
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Function	X		62.5mA/LSB													

READ_TEMPERATURE_1 (8Dh)

The READ_TEMPERATURE_1 command returns 10-bit external sensed temperature, in degrees Celsius. READ_TEMPERATURE_1 is a paged command. The default value is 0x0019.

Command						READ_ TEMPERATURE_1									
Format						Direct, 2's complement									
Default						25°C (0x0019)									
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Function	X					1°C/LSB										

READ_TEMPERATURE_2 (8Eh)

The READ_TEMPERATURE_2 command returns 10-bit ES5201 internal sensed temperature, in degrees Celsius. READ_ TEMPERATURE_2 is not a paged command. The default value is 0x0019.

Command						READ_ TEMPERATURE_2									
Format						Direct, 2's complement									
Default						25°C (0x0019)									
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Function	X					1°C/LSB										

PMBUS_REVISION (98h)

The PMBUS_REVISION command returns the protocol revision used. Accesses to this command should use the read byte protocol. Bit [7:4] indicates the PMBus revision of specification Part I to which the device is compliant. Bit [3:0] indicates the revision of specification Part II to which the device is compliant.

Bit [7:4] is always read as 4'b0011, specification PMBus Part I Revision 1.3.

Bit [3:0] is always read as 4'b0011, specification PMBus Part II Revision 1.3.

MFR_DEVICE_ID (99h)

The MFR_DEVICE_ID command report the device ID which is 0x80 for ES5201. This read only commands has one data byte. It is not a paged command.

MFR_PIN_SETTING (9Ah)

The MFR_PIN_SETTING command reports the ILMT, RT pin setting. It is not a paged command. This read only commands has one data byte.

BIT	VALUE	MEANING
7	1	EN1 pin is logic high
6	1	EN0 pin is logic high
5	1	Channel 1 is in forced DCM mode
4	1	Channel 0 is in forced DCM mode
3	1	SYNC pin is programmed as SYNC IN
2:0	000	ILMT pin sets VCSMAX to 24mV
	001	ILMT pin set VCSMAX to 12mV
	010	ILMT pin set VCSMAX to 36mV
	011	ILMT pin set VCSMAX to 48mV
	100	ILMT pin set VCSMAX to 60mV

MFR_IOUT_CAL_GAIN_TC(B1h)

The MFR_IOUT_CAL_GAIN_TC command allows the user to program the temperature coefficient of the IOUT_CAL_GAIN sense resistor or inductor DCR in ppm/°C. It is a paged command. This command has one data byte. The IOUT_CAL_GAIN is multiplied by [1.0 + MFR_IOUT_CAL_GAIN_TC • (READ_TEMPERATURE_1-25)].

DCR sensing will have a typical value of 3900ppm/°C (0.0039/°C, 0x27). The valid range of the command is between 0x24(0.0036/°C) and 0x2B(0.0043/°C). If a host sends a value out of this range, the ES5201 rejects the command. It is not a paged command.

Command	MFR_IOUT_CAL_GAIN_TC							
Format	Direct, unsigned							
Default	0x27							
Bit	7	6	5	4	3	2	1	0
Function	X	0.0001°C / LSB						

MFR_VIN_PEAK(BBh)

The MFR_VIN_PEAK command reports the highest volt age, in volts, reported by the READ_VIN measurement. To clear the peak value and restart the peak monitor, use the MFR_CLEAR_PEAKS command. This command has two data bytes and is formatted as a 14-bit unsigned binary integer scaled 8mV/ bit. The MFR_VIN_PEAK is not a paged command.

MFR_VOUT_PEAK (ABh)

The MFR_VOUT_PEAK command reports the highest voltage, in volts, reported by the READ_VOUT measurement. To clear the peak value and restart the peak monitor, use the MFR_CLEAR_PEAKS command. This command has two data bytes and is formatted as a 14-bit unsigned binary integer scaled 1mV/ bit. The MFR_VOUT_PEAK is a paged command.

MFR_IOUT_PEAK (BCh)

The MFR_IOUT_PEAK command reports the highest current, in amperes, reported by the READ_IOUT measurement. To clear the peak value and restart the peak monitor, use the MFR_CLEAR_PEAKS command. This command has two data bytes and is formatted as a 14-bit 2's complement value scaled 62.5mA/bit. The MFR_IOUT_PEAK is a paged command.

MFR_TEMPERATURE_1_PEAK (BDh)

The MFR_TEMPERATURE_1_PEAK command reports the highest temperature, in degrees Celsius, reported by the READ_TEMPERATURE_1 measurement. Its LSB is 1°C. This command is cleared using the MFR_CLEAR_PEAKS command. It is a paged command.

MFR_TEMPERATURE_2_PEAK (BEh)

The MFR_TEMPERATURE_2_PEAK command reports the highest temperature, in degrees Celsius, reported by the READ_TEMPERATURE_2 measurement. Its LSB is 1°C. This command is cleared using the MFR_CLEAR_PEAKS command. It is not a paged command.

MFR_CLEAR_PEAKS (BFh)

The MFR_CLEAR_PEAKS command clears the MFR_*_PEAK data values and restarts the peak monitor routine. This write-only command requires no data bytes but will accept and ignore up to two bytes. It is not a paged command.

MFR_VOUT_SLEW_RATE (C7h)

The MFR_VOUT_SLEW_RATE controls the slew rate of current DAC which is used to offset the output. This one-byte command has four valid bits which is shown as below.

The default value for this command is 0x00. MFR_VOUT_SLEW_RATE is a paged command.

[3:0]	Switching Clock	[3:0]	Switching Clock
0000	1024	1000	256
0001	2	1001	1024
0010	4	1010	2048

[3:0]	Switching Clock	[3:0]	Switching Clock
0011	8	1011	4096
0100	16	1100	4096
0101	32	1101	4096
0110	64	1110	4096
0111	128	1111	4096

MFR_ADDRESS (C9h)

The MFR_ADDRESS command reports the 7-bit PMBus address set by the ADDR1 and ADDR0 pins.

MFR_RAIL_ADDRESS (CAh)

The MFR_RAIL_ADDRESS command enables direct device address access to the PAGE activated channel. The value of this command should be common to all devices attached to a single power supply rail. Users should only perform command writes to this address. The MSB (BIT [7]) must be set high to enable communication using the MFR_RAIL_ADDRESS address. Setting this command to a value of 0x00 disables rail device addressing for the channel. It is a paged command.

This command has one data byte. Its default value is 0x00.

BIT	VALUE	MEANING
7	1	Enable the MFR_RAIL_ADDRESS
	0	Disable the MFR_RAIL_ADDRESS
6:0		7-Bit MFR_RAIL_ADDRESS address

MFR_SETTING (CBh)

One-byte setting command to set the ES5201 operation condition.

BIT	VALUE	MEANING
7:5		Reserved
4	1	Double the ADC Sampling Rate
3	1	Enable Method B Transient Improvement Circuit
2	1	Enable Method A Transient Improvement Circuit
1	1	Program Page1 to DCM
0	1	Program Page0 to DCM

MFR_SMBALERT_MASK (CCh)

This command provides a means by which the user can mask the ALERTB signal.

BIT	VALUE	MEANING
7:1		Reserved
0	1	Mask the CML to the ALERTB pin

MFR_RESET (CFh)

This command provides a means by which the user can perform a reset of the ES5201 PMBus interface and ADC. Write to this command to reset PMBus interface and ADC to power-on state. Write data is ignored.

DESIGN EXAMPLE

Figure 7 shows an ES5201 design in a dual output configuration. The typical input voltage is 12V. The channel 0 output is 1.2V and the channel 1 output is 1.8V. Both output current is 25A.

The channel 0 output is set by:

$$V_{OUT} = 0.5V \cdot (1+ \frac{R_A}{R_B}) = 0.5V \cdot (1+ \frac{28k\Omega}{20k\Omega}) = 1.2V$$

The channel 1 output is set by:

$$V_{OUT} = 0.5V \cdot (1+ \frac{R_A}{R_B}) = 0.5V \cdot (1+ \frac{52.3k\Omega}{20k\Omega}) \approx 1.8V$$

Selecting the switching frequency is a tradeoff between solution size and efficiency. High switching frequency helps to reduce the solution size by using smaller output capacitors and inductors. However, it causes extra switching losses. For this application, 400kHz is selected by connecting the RT pin to ground.

For peak current mode control application, the typical inductor current ripple is between 20% and 40% of the maximum output current. The inductor value can be calculated if 25% is chosen as:

$$L = \frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{V_{IN} \cdot F_S \cdot 0.25 \cdot I_{OUT}}$$

$$= \frac{1.2V \cdot (12V - 1.2V)}{12V \cdot 400kHz \cdot 0.25 \cdot 25A}$$

$$= 0.432\mu H$$

Choose 0.47µH (0.67mΩ DCR) Wurth 744355147 inductor for both channels to ease the design. A 0.1µF capacitor and a 7.15kΩ resistor are chosen as the DCR sensing network for current sense purpose.

To leave some design margin, the maximum current sense threshold is set to 36mV by floating the ILMT pin.

A 4.7µF capacitor is connected to the V_{INT} pin to stabilize the V_{INT} output. Each SS pin has 0.1µF capacitor for external soft-start purpose. There is 0.1µF capacitor between each channel's BST and LX pins to store the energy to turn on the top Power MOSFET.

TYPICAL APPLICATIONS

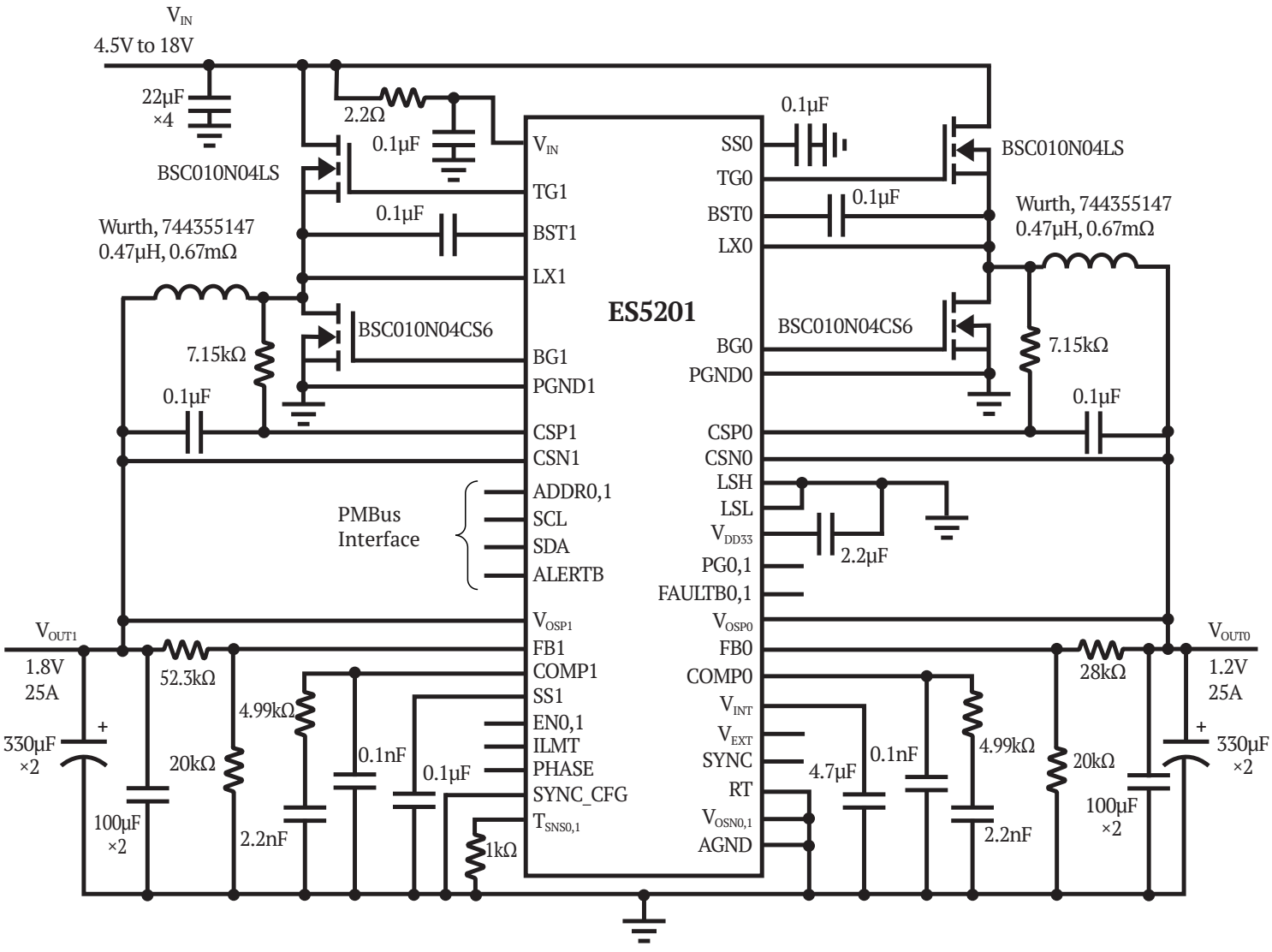


Figure 7 High Efficiency 400kHz Dual 1.2V/1.8V Output Step-Down Converter

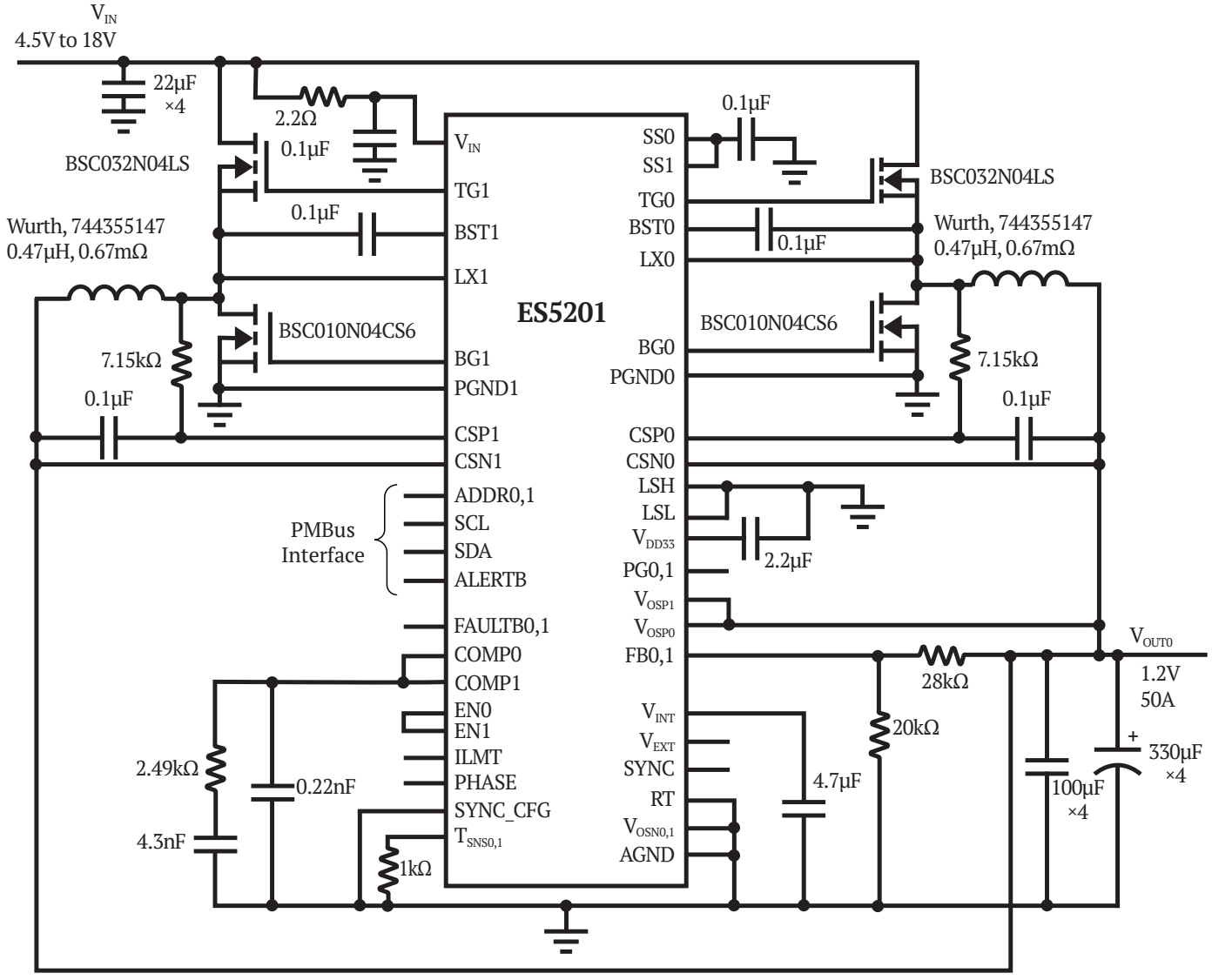


Figure 8 High Efficiency 400kHz Dual-Phase 1.2V/50A Output Step-Down Converter

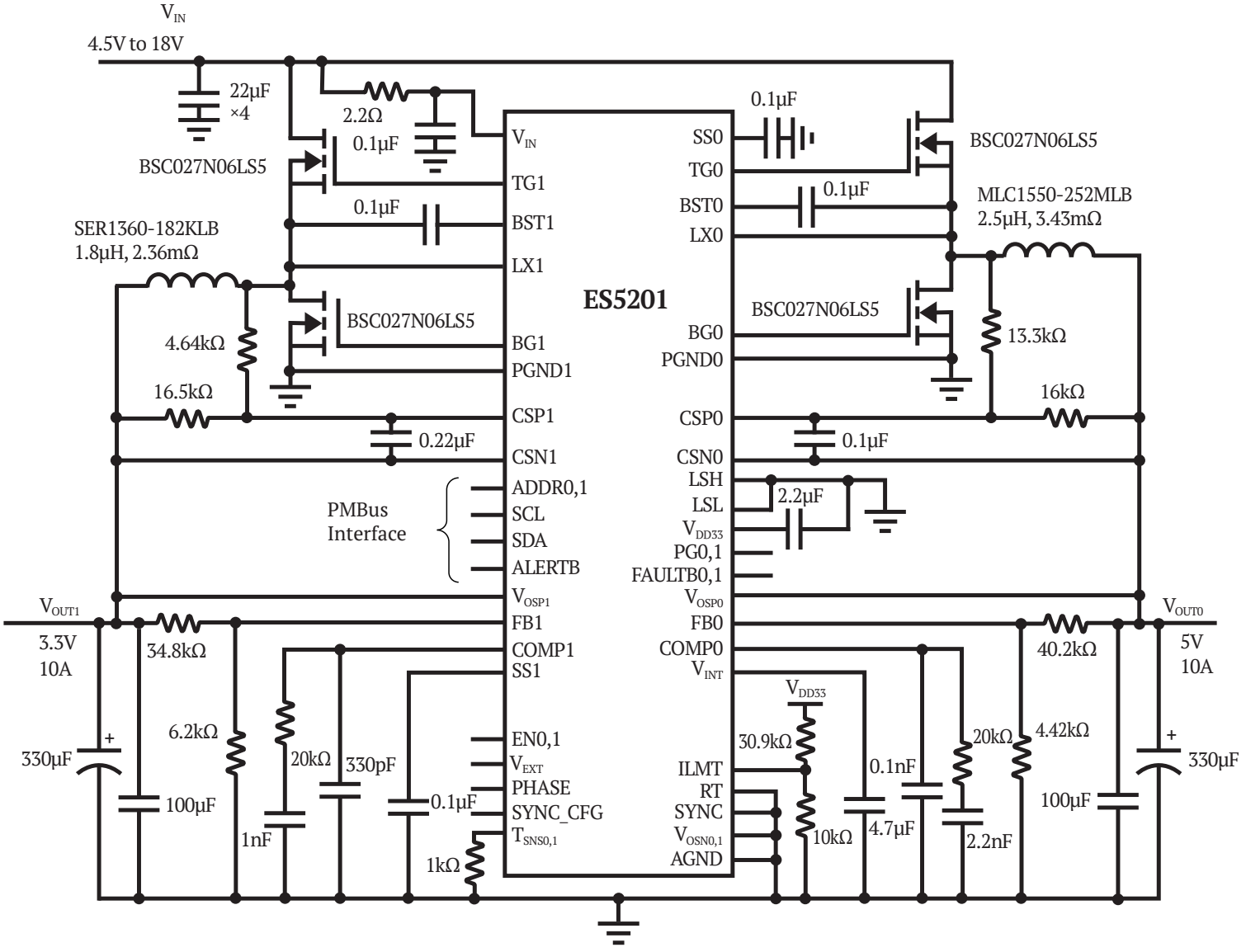
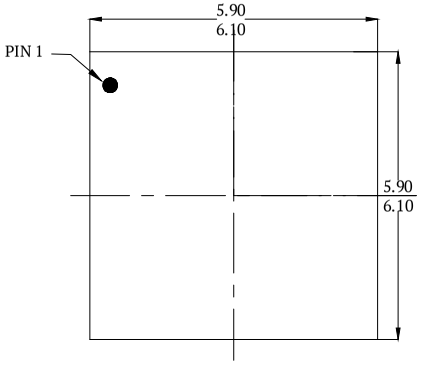


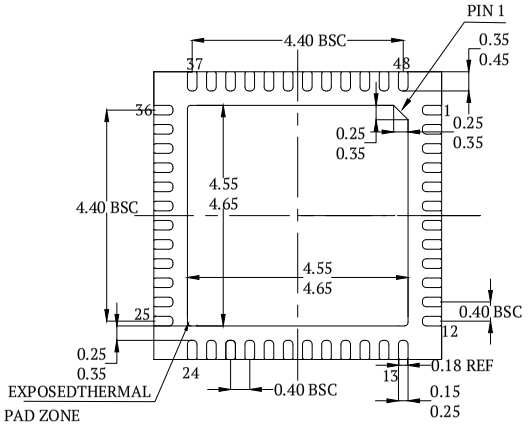
Figure 9 High Efficiency 400kHz Dual 5V/3.3V Output Step-Down Converter

PACKAGE OUTLINE DRAWING

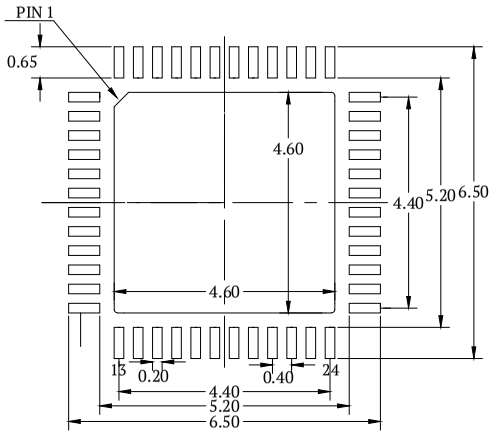
QFN PACKAGE
48-LEAD 6.00mm × 6.00mm × 0.75mm
POD-0010-A2
Unit: mm



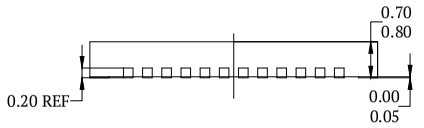
TOP VIEW



BOTTOM VIEW

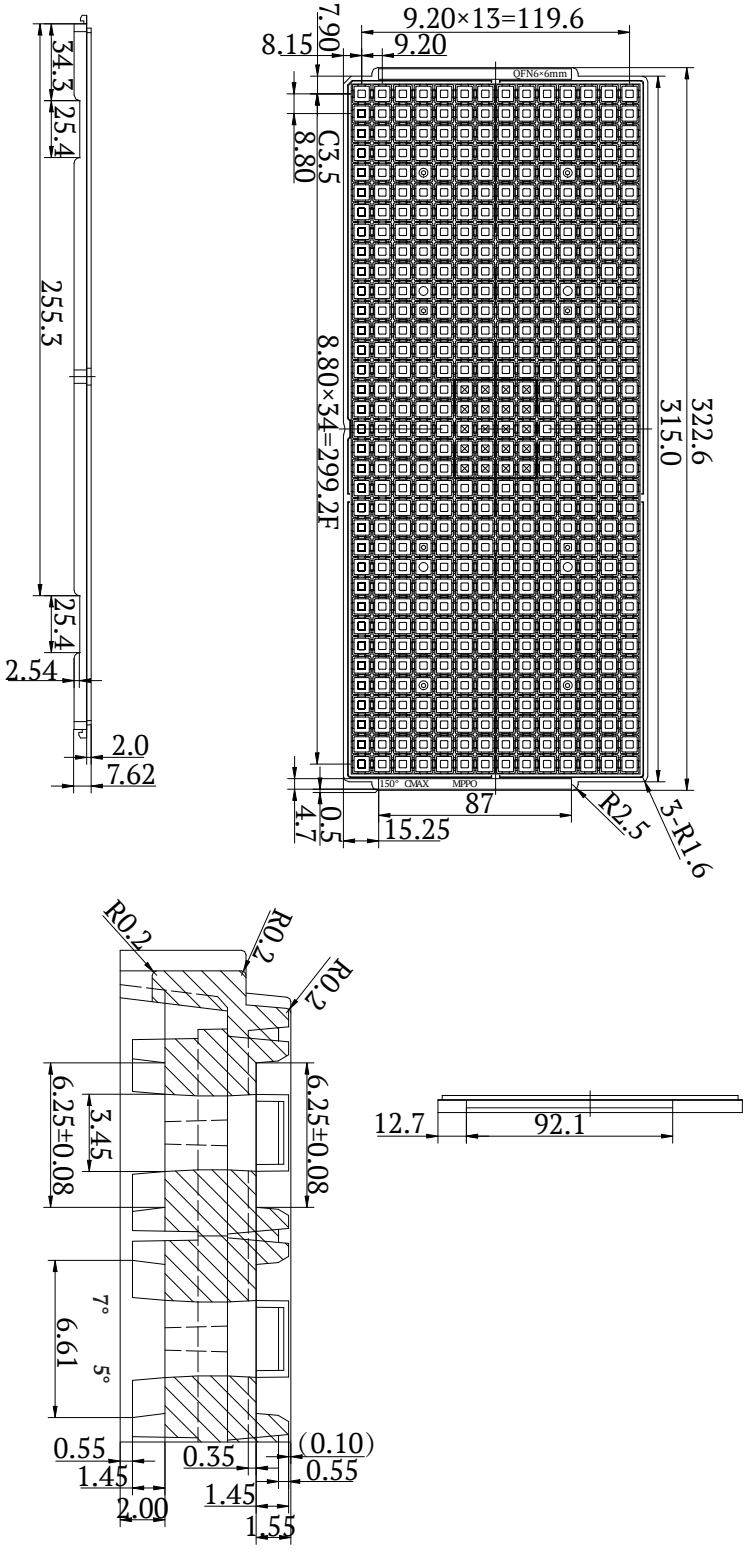


RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



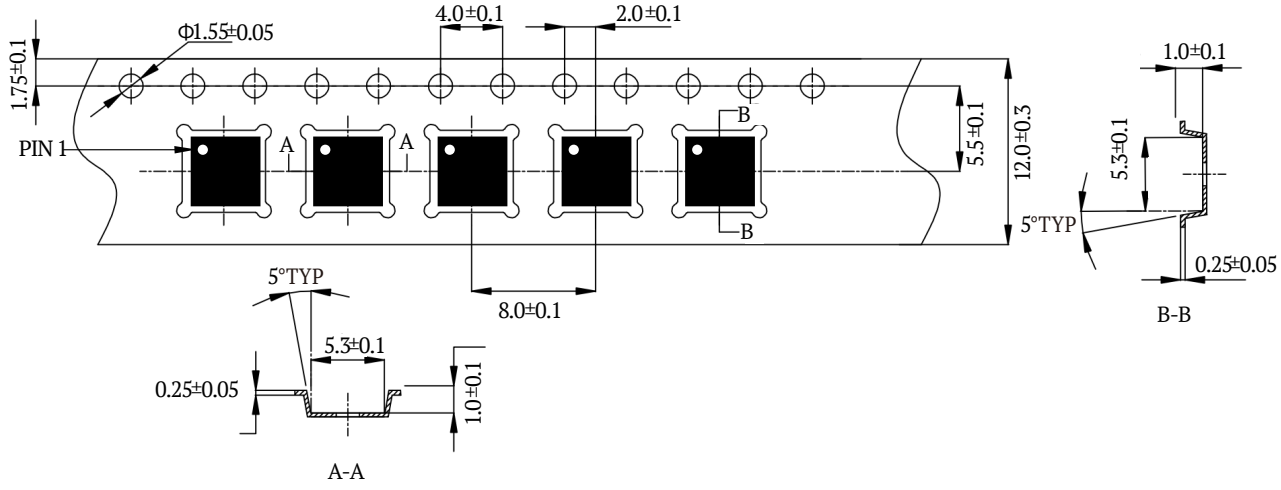
SIDE VIEW

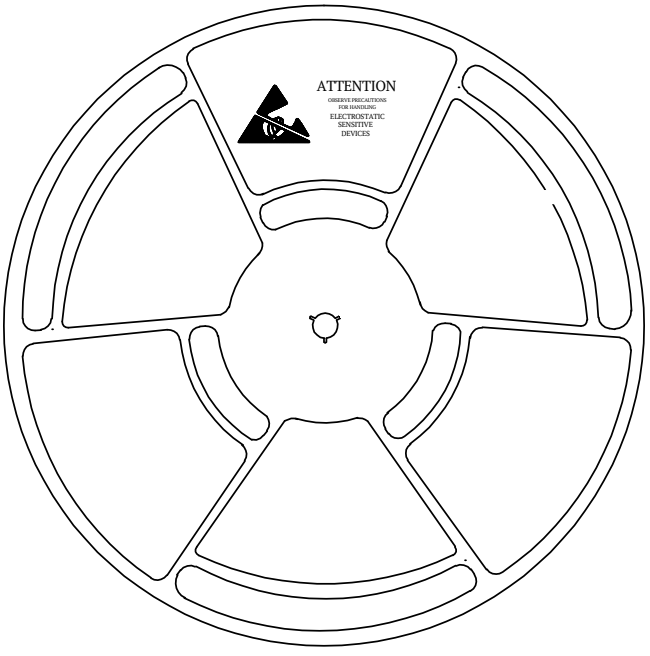
PACKING MATERIAL (TRAY)



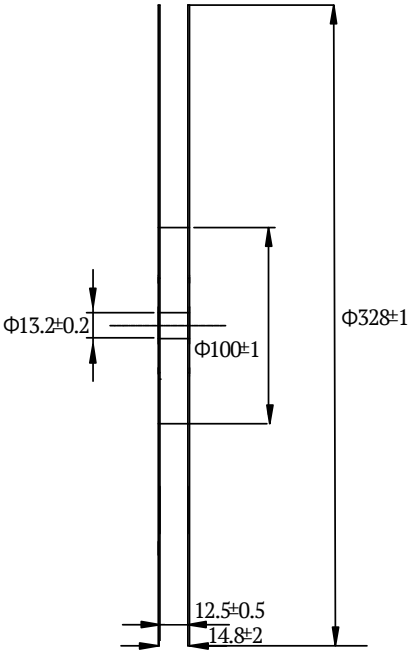
PART NO.	PMT 0010
TRAY TYPE	6.25×6.25×1.45mm
QTY	490 ea/Pcs
UNIT SIZE	mm

PACKING MATERIAL (TAPE & REEL)





SCALE: 1:1



SECTION A-A

NOTE:

1. Unit Size: mm
2. SPQ: 3000 PCS