20A Synchronous Buck Regulator with PMBus Interface

DESCRIPTION

The ES5325 is an easy-to-use, fully integrated and highly efficient switching mode DC/DC Regulator with PMBus compliant serial interface. Operating over a wide input range of 4.5V to 17V, the ES5325 support up to 20A of output current per phase with an accurate 0.5V reference and excellent load and line regulation.

The ES5325 features remote configurability and telemetry-monitoring of power management parameters over PMBus interface. It supports differential remote sensing amplifier, multi-phase parallel with accurate current sharing, external frequency synchronization and output voltage tracking for rail sequencing.

Fault protection includes overvoltage, overcurrent and overtemperature protection. The ES5325 is offered in a high density and thermally enhanced 5mm×6mm×1.4mm LQFN package with RoHS compliant terminal finish.

APPLICATIONS

- CPU and Memory Voltage Regulators
- High-Current Utility Rails in Server System
- Communications Infrastructure Equipment

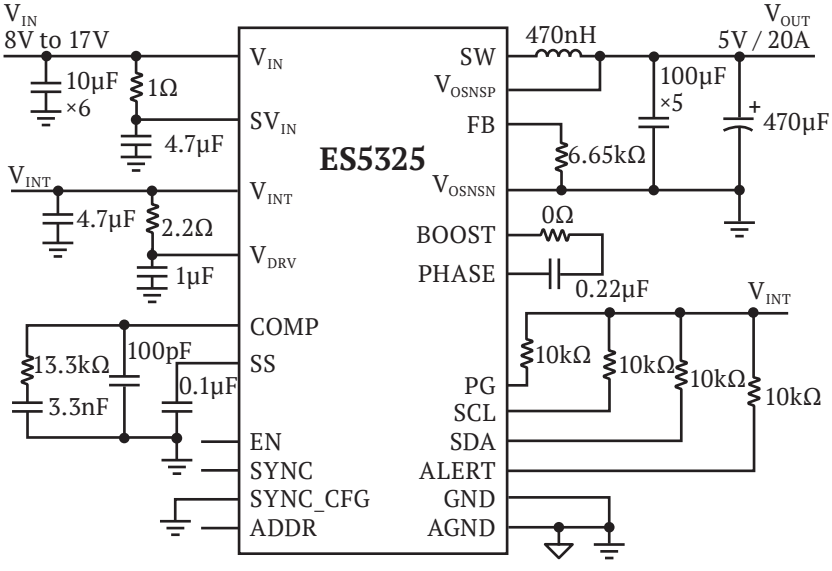
FEATURES

- Wide Input Voltage Range: 4.5V to 17V
- Wide Output Voltage Range: 0.5V to 5.5V
- 20A Output Current Capability
- PMBus Compliant Serial Interface
  -Telemetry Read-Back: V_{IN}, V_{OUT}, Temperature
  -Program V_{OUT}, OV/OC/OT Warning
- Overcurrent Protection
- Programmable Soft-Start with Output Pre-Biased Function
- Input Overvoltage Lockout (OVLO) Protection
- Differential Remote Sensing Amplifiers
- Power Good Indicator
- Thermal Shutdown for Overtemperature Protection
- 5mm × 6mm × 1.4mm LQFN Package

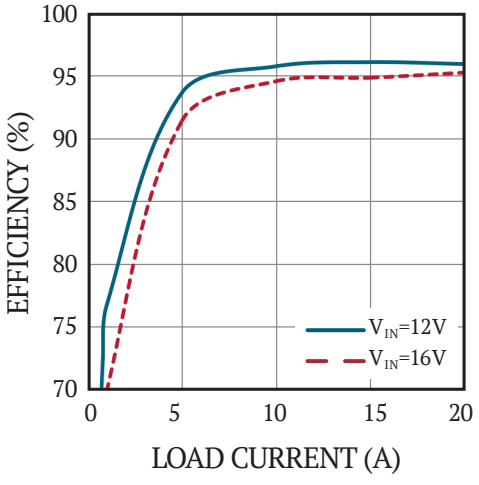
PART NUMBER	OUTPUT VOLTAGE	OUTPUT CURRENT	PACKAGE
ES5340	0.5V-2V	40A	37-LEAD 5mm×6mm× 1.4mm LQFN Package
ES5335	0.5V-3.6V	30A	
ES5325	0.5V-5.5V	20A	

TYPICAL APPLICATION

8V to 17V Input, Single 20A Outputs DC/DC Regulator

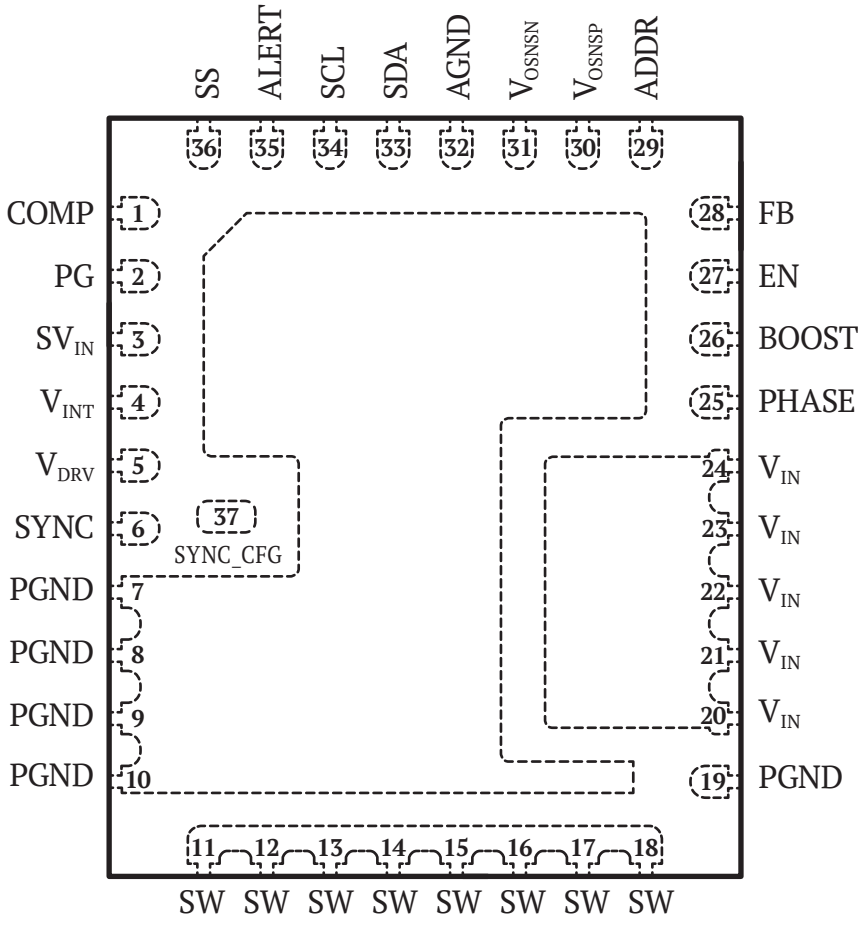


Efficiency at 5V Output Voltage



PIN CONFIGURATION AND FUNCTIONS

TOP VIEW



37-LEAD 5mm × 6mm × 1.4mm LQFN Package
T_{JMAX} = 125°C, Weight = 0.107g

PIN#	PIN Name	PIN Description
1	COMP	Current Control Threshold and Error Amplifier Compensation Pin. The current comparators' threshold increases with this pin.
2	PG	Output Voltage Power Good Indicator. Open drain logic output that is pulled to ground when either output voltage is not within ±10% of the regulation point.
3	SV_{IN}	Input Voltage For an Internal LDO. A 4.7μF capacitor should be connected between this pin and PGND.
4	V_{INT}	Internal 5V LDO Output. The control circuits are biased from this voltage. Decouple this pin to PGND with a minimum of 4.7μF low ESR ceramic or tantalum capacitor.
5	V_{DRV}	The Gate Driver Power Supply Pin. Decouple this pin to PGND with a minimum of 1μF capacitor.

PIN#	PIN Name	PIN Description
6	SYNC	Switching Frequency Synchronization Pin. It can be programmed as SYNC IN or SYNC OUT by the SYNC_CFG pin. Do not float the SYNC pin when set to SYNC IN.
7-10, 19	PGND	Power Ground Pins.
11-18	SW	Inductor Pins. Connect these pins to the switching node of inductor.
20-24	V_{IN}	Main Input Supply Pins. Decouple these pins to PGND with capacitors.
25	PHASE	Internal Connection to the High-side MOSFET Source Pin. For Bootstrap capacitor connection only.
26	BOOST	Bootstrap Pin. Supply high side gate driver.
27	EN	Enable Pins. Pull low below 1.16V to disable the device and pull high above 1.22V to enable this device. There is a 1μA pull-up current for this pin. Once the EN pin rises above 1.22V, an additional 1μA pull-up current is added to the pin.
28	FB	The Negative Input of the Error Amplifier for Channel. Internally, These pins are connected to V_{OSNSP} with a 60.4kΩ precision resistor. Different output voltages can be programmed with an additional resistor between FB and AGND pins. In multi-phase operation, tying the FB pins together allows for parallel operation. See the Applications Information section for details.
29	ADDR	PMBus Address Select Pin. A resistor between AGND to this pin to set the 4 LSB PMBus address.
30	V_{OSNSP}	Positive Output Voltage Sense Input. Connect this pin to the positive side of the output voltage sense point
31	V_{OSNSN}	Negative Inputs of Remote Sensing Amplifiers. Connect this pin directly to the negative side of the output voltage sense point.
32	AGND	Analog Ground Pin.
33	SDA	Serial Bus Data Input and Open-Drain Output. A pull-up resistor is required in the application.
34	SCL	Serial Bus Clock Pin.
35	ALERT	PMBus Alert Pin. A pull-up resistor is required for this open drain output pin.
36	SS	External Soft-Start Voltage Pins. There is a 1μA pull-up current for this pin. Soft-start time can be adjusted by adding an appropriate external capacitor between this pin and AGND.
37	SYNC_CFG	SYNC Configuration Pin. When the SYNC_CFG pin is floating, the SYNC pin is programmed as SYNC IN; when the SYNC_CFG pin is tied to AGND, the SYNC pin is programmed as SYNC OUT.

ORDER INFORMATION

PART NUMBER	FINISH	MARKING	PACKAGE TYPE	PACKING MATERIAL	MSL	TEMPERATURE RANGE
ES5325IW#PBF	Au(RoHS)	5325	LQFN	TRAY	3	-40°C to 125°C
ES5325IW#TRPBF	Au(RoHS)	5325	LQFN	TAPE&REEL	3	-40°C to 125°C

ABSOLUTE MAXIMUM RATINGS (Note 1)

	MIN	TYP	MAX	UNITS
Terminal Voltage				
SV_{IN}, V_{IN}	4.5		24	V
BOOST	-0.3		V_{IN}+6	V
SW, PHASE	GND-5		V_{IN}	V
V_{INT}, V_{DRV}, EN, ALERT, V_{OSNSP}	-0.3		6	V
V_{OSNSN}, SS, FB, COMP, SYNC_CFG, SYNC, ADDR, SCL, SDA, AGND, PGND, PG	-0.3		V_{INT}	V
Temperatures				
Junction Temperature (Note 2)	-40		150	°C
Storage Temperature Range	-65		150	°C
Peak Solder Reflow Package Body Temperature		260		°C

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Electrical Characteristics. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
Note 2: Operating at junction temperatures greater than 125°C, although possible, degrades the lifetime of the device.

ESD RATINGS

	VALUE	UNIT
HBM (Human Body Model)	2	kV
CDM (Charged Device Model)	1	kV

Note: JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process. JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

ELECTRICAL CHARACTERISTICS

The Y denotes the specifications which apply T_A = -40°C to +125°C Full Temperature Range (FTR) (Note 3). Typical values are at T_J = 25°C. V_{IN} = SV_{IN} = 12V, V_{INT} = V_{DRV} = 5V unless otherwise specified. The values are guaranteed by test, design or statistical correlation.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	FTR
Input DC Voltage	V_{IN}, SV_{IN}		4.5		17	V	Y
V_{DRV} UVLO Rising Threshold	$V_{VDRV, UVLO}$		3.7	3.85	4.1	V	
V_{DRV} UVLO Hysteresis	$V_{VDRV, HYS}$			0.4		V	
$R_{DS(ON)}$	$R_{DS(ON)\_TOP}$ $R_{DS(ON)\_BOT}$	(Note 5) (Note 5)		3.4 1		mΩ mΩ	
Dead-Time	T_{DEAD}	SW Rising (Note 4)		1		ns	
SW Bleeding Resistor	R_{SW}			0.3		kΩ	
Regulated Feedback Voltage	V_{FB}		495	500	505	mV	Y
Resistor Between V_{OSNSP} and FB Pin	R_{FB}		59.80	60.40	60.75	kΩ	
Feedback Current	I_{FB}	(Note 5)	-60		60	nA	
Reference Voltage Line Regulation	$V_{REFLINEREG}$	SV_{IN} = 4.5V to 17V (Note 5)		0.002	0.005	%/V	
Output Voltage Load Regulation	$V_{LOADREG}$	Measured in Servo Loop Δ_{COMP} Voltage = 1.2V to 1.7V (Note 5)		0.01	0.1	%	
Transconductance Amplifier g_m	g_m	COMP = 1.2V, Sink/Source 5µA (Note 5)		2		mmho	
Feedback Overvoltage Lockout	V_{OVLK}	Measured at FB	0.53	0.55	0.57	V	Y
V_{OSNSP} Input Impedance	R_{VOSNSP}	V_{EN} = 5V (Note 5)		96		kΩ	
SV_{IN} Quiescent Current	I_{Q_SVIN}	V_{EN} = 0V V_{EN} = 5V		6 8		mA mA	
EN Rising Threshold	V_{EN_R}		1.18	1.22	1.26	V	
EN Threshold Hysteresis	V_{EN_HYS}			60		mV	
SS Charge Current	I_{SS}	V_{SS} = 0V	0.8	1	1.2	µA	Y
Current DAC Accuracy	$I_{DAC1, 2}$	VOUT_COMMAND=0x007F VOUT_COMMAND=0x0080	62.5 -65	63.5 -64	64.5 -63	µA µA	Y Y
Current DAC LSB				0.5		µA	
V_{INT} Regulator Output Voltage	V_{INT}	I_{VINT} = 0mA		5.0		V	
Output Current Limit	I_{OUT_PK}	(Note 4)	23			A	

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	FTR
V_{INT} Load Regulation	V_{INT_REG}	I_{VINT} = 20mA		0.5	2	%	
V_{INT} UVLO Rising Threshold	$V_{VINT, UVLOR}$		3.9	4.1	4.3	V	
V_{INT} ULVO Falling Threshold	$V_{VINT, UVLOF}$			3.8		V	
Power Good Threshold	V_{PG}	FB with Respect to Set Output Voltage FB Ramping Down FB Ramping Up		 -10 10		 % %	
PG Pin Leakage Current	I_{PG}	V_{PG} = 5V	-2		2	µA	Y
Power Good Delay	t_{PG_F}	High to low (Note 5)		60		µs	
SWITCHING FREQUENCY AND PLL							
Switching Frequency	F_S			600		kHz	
CH0 to SYNC Phase Relationship, SYNC IN				90		Deg	
Synchronizable Frequency Range		SYNC Pin = External Clock	200		1300	kHz	
SYNC Pin High Level		SYNC_CFG Pin = 5V	2.2			V	
SYNC Pin Low Level		SYNC_CFG Pin = 5V			0.5	V	
ADC READBACK							
SV_{IN} Readback LSB	V_{INLSB}			8		mV	
SV_{IN} Readback Range	V_{INRG}			17		V	
SV_{IN} Readback Accuracy	V_{INACC}		-2		+2	%	Y
V_{OUT} Readback LSB	V_{OUTLSB}			1		mV	
V_{OUT} Readback Range	V_{OUTRG}			2		V	
V_{OUT} Readback Accuracy	V_{OUTACC}		-2		+2	%	Y
Output Current Readback Accuracy	I_{OUTACC}	I_{OUT} = 10A		10		A	
PMBUS DC CHARACTERISTICS							
SCL, SDA Logic High Voltage	$V_{IH, PMBUS}$		1.4			V	
SCL, SDA Logic Low Voltage	$V_{IL, PMBUS}$				0.4	V	
Leakage Current SCL, SDA, ALERTB			-2		2	µA	
SDA Pull Down Resistance	R_{SDA}			55	150	Ω	
ALERTB Pull Down Resistance	R_{ALERTB}			75	200	Ω	

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	FTR
PMBUS TIMING CHARACTERISTICS							
PMBus Operating Frequency	f_{SCL}		10		1000	kHz	
Bus Free Time	t_{BFT}	Between Stop and Start Condition	1.3			µs	
Hold Time	t_{HT}		0.6			µs	
Repeated Start Condition Setup Time			0.6			µs	
Stop Condition Setup Time			0.6			µs	
Data Hold Time	t_{DH}		0.3			µs	
Data Setup Time	t_{DS}		0.1			µs	
Clock Low Period	t_{LOW}		1.3			µs	
Clock High Period	t_{HIGH}		0.6			µs	

Note 3: The ES5325 is tested under pulsed load conditions such that $T_J \approx T_A$. The ES5325I is guaranteed over the full –40°C to 125°C internal operating temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

Note 4: Guaranteed by design and characterization, not tested in production.

Note 5: These parameters are tested at wafer sort.

BLOCK DIAGRAM

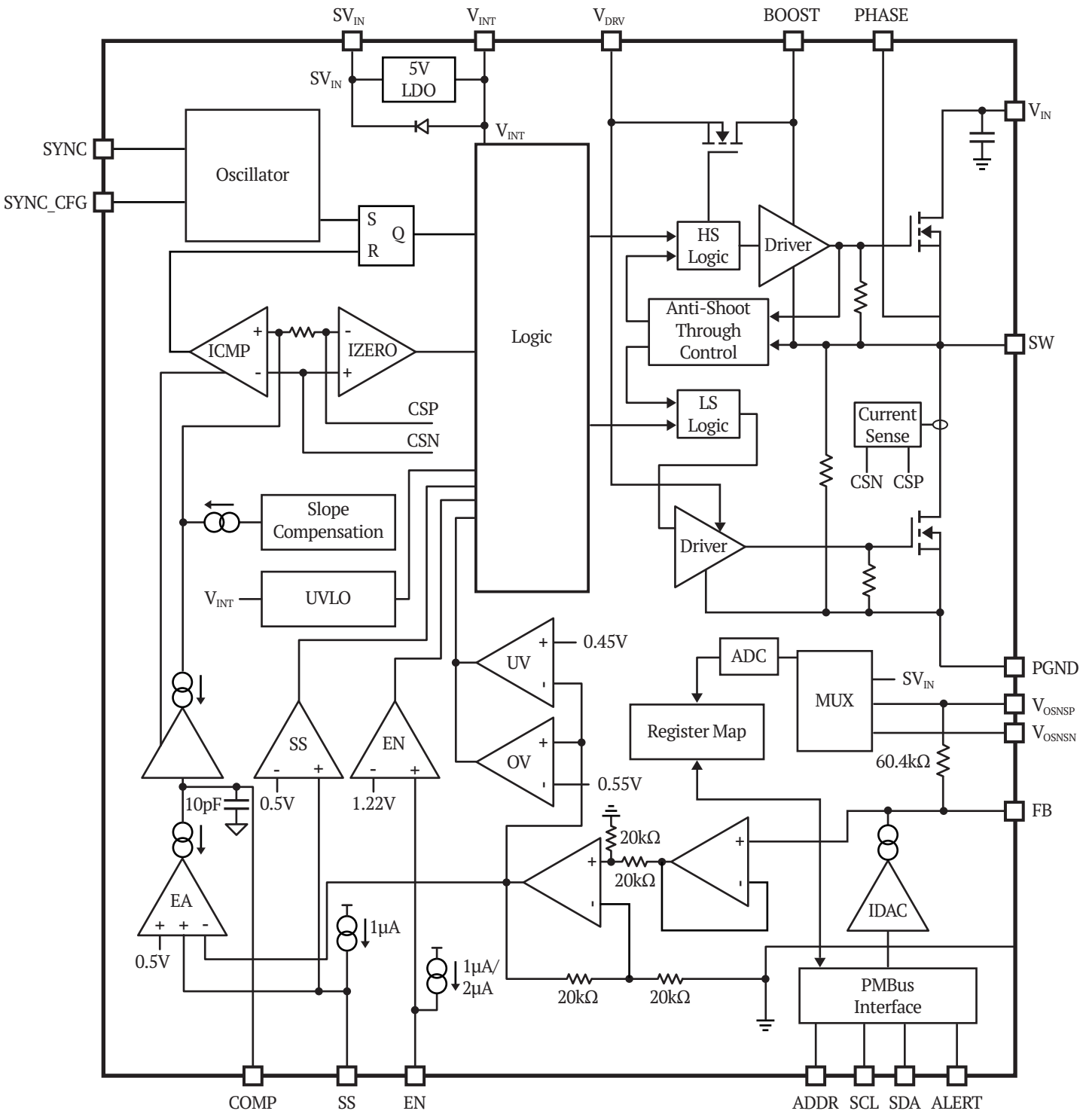
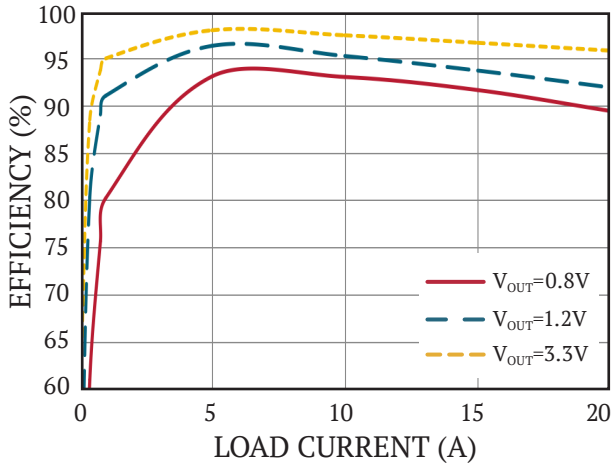


Figure 1 Simplified ES5325 Internal Function Block Diagram

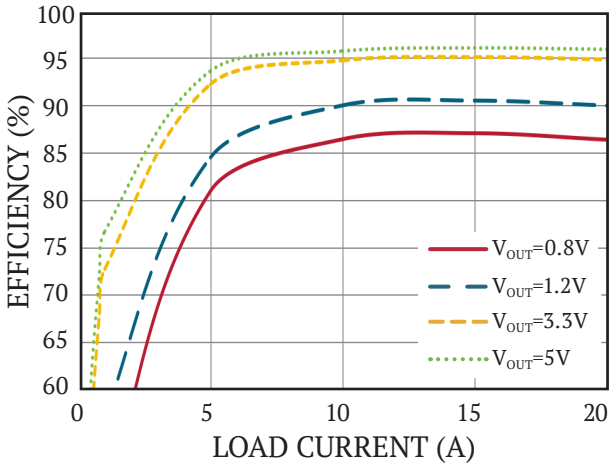
TYPICAL PERFORMANCE CHARACTERISTICS

Efficiency vs Load Current From 5V Input



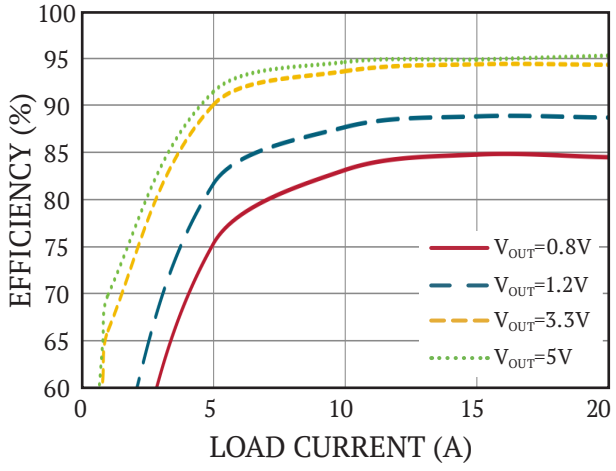
L=0.47μH, F_S=600kHz

Efficiency vs Load Current From 12V Input



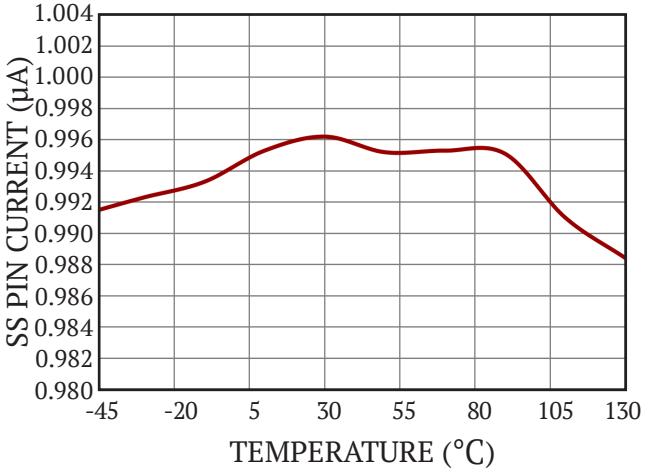
L=0.47μH, F_S=600kHz

Efficiency vs Load Current From 16V Input

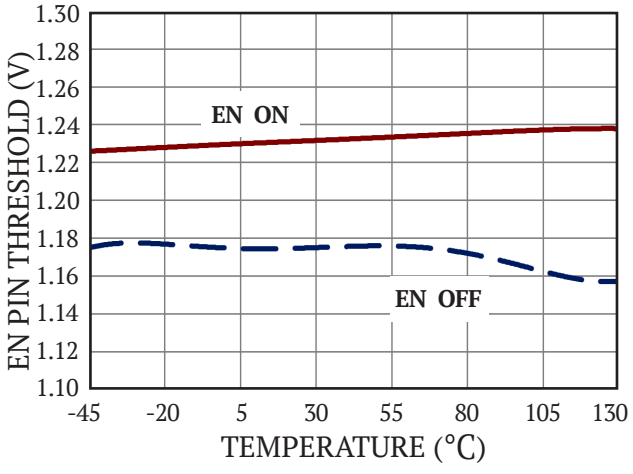


L=0.47μH, F_S=600kHz

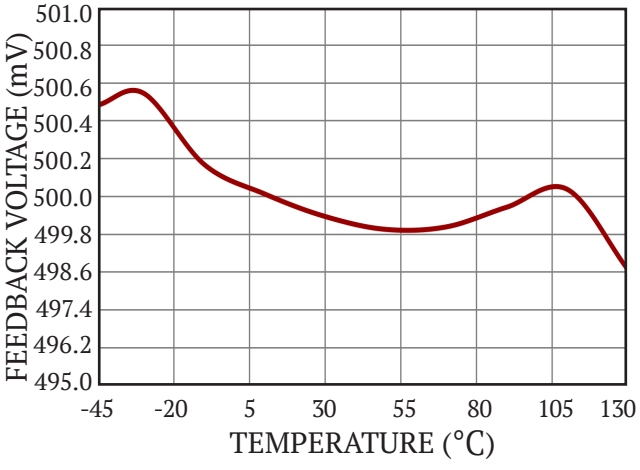
SS Pin Pull-Up Current vs Temperature



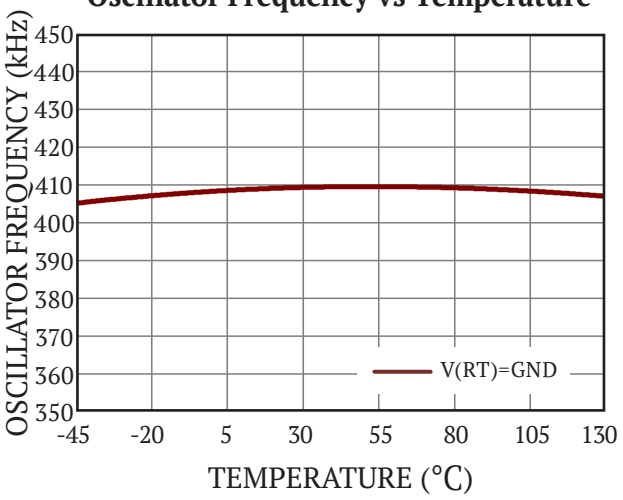
EN Pin Threshold vs Temperature



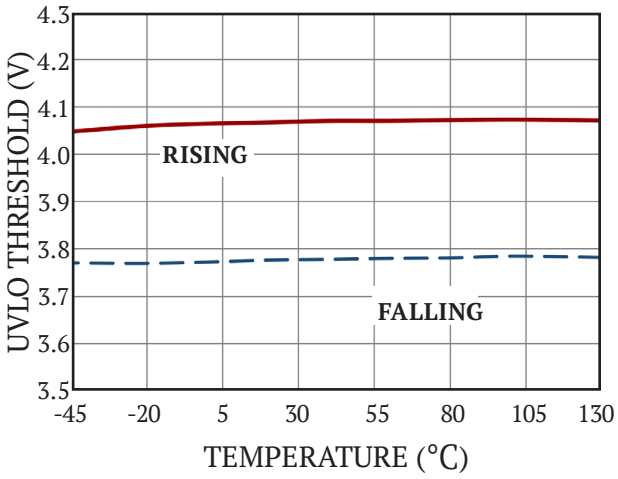
Regulated Feedback Voltage vs Temperature



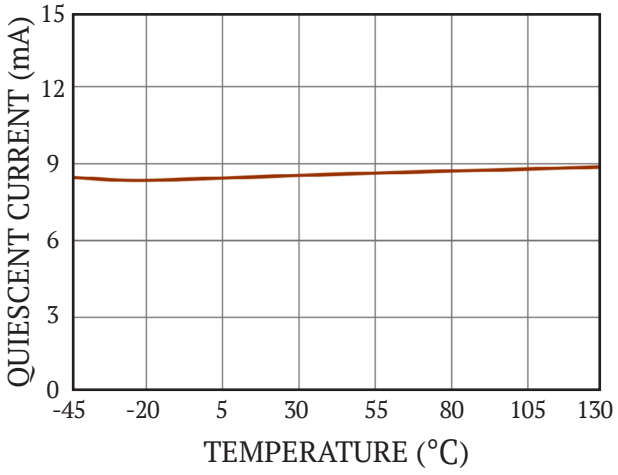
Oscillator Frequency vs Temperature



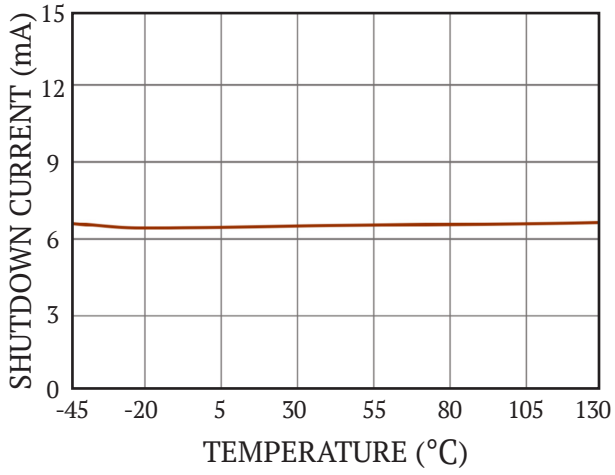
UVLO vs Temperature



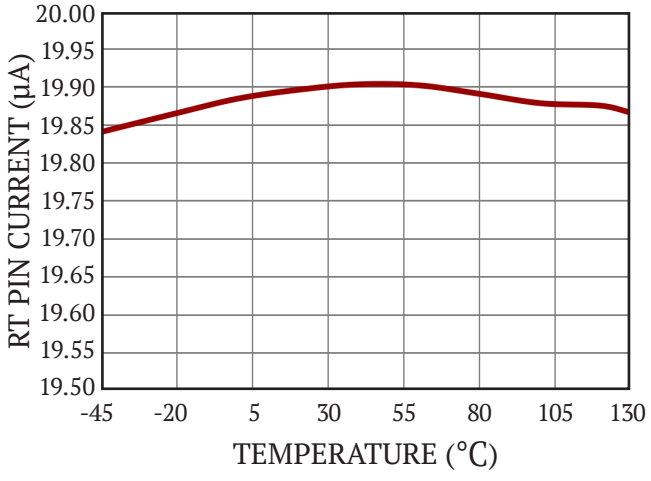
Quiescent Current vs Temperature



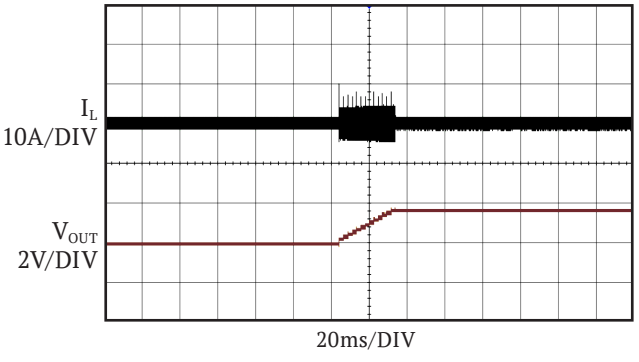
Shutdown Current vs Temperature



RT Pin Current vs Temperature

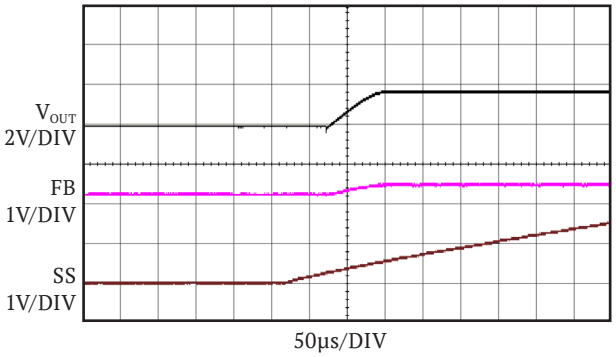


Output Program via PMBus Interface



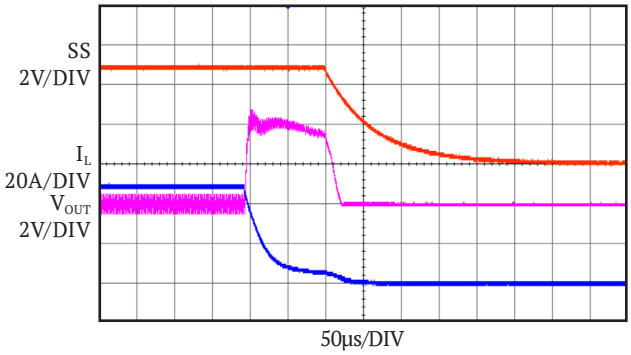
F_S=400kHz
V_{IN}=12V
V_{OUT}=1.8V

Start-up into a Prebiased Output



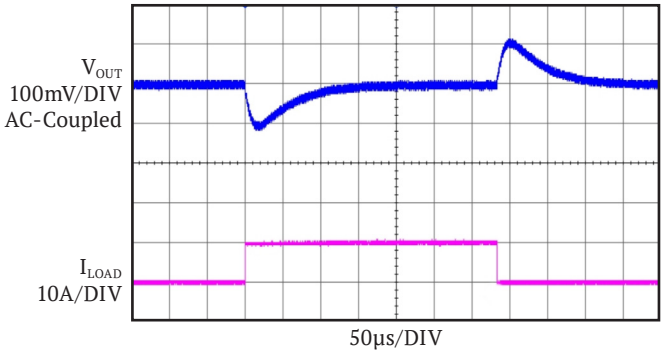
V_{IN}=12V,
V_{OUT}=1.8V

64-Cycle Overcurrent Counter to Hiccup



V_{IN}=12V, V_{OUT}=5V

Load Step (FCCM)



V_{IN}=12V, V_{OUT}=5V, F_S=600kHz
0A to 10A LOAD STEP
C_{OUT}=4×100μF CERAMIC CAP + 47μF CERAMIC CAP + 2×220μF POSCAP

DETAILED DESCRIPTION

GENERAL FEATURES

The ES5325 is an easy-to-use, fully integrated and highly efficient DC/DC Regulator with PMBus compliant serial interface. It achieves 20A of continuous output current over a wide input range from 4.5V to 17V.

It uses peak current mode control architecture for easy loop compensation, excellent line and load regulation, and flexible phase extension.

Adaptive dead-time control and driver's UVLO allow system optimization for high efficiency and reliability.

ENABLE CONTROL

The ES5325 has precision enable control inputs. When channel EN pin voltage is greater than 1.22V, that channel is enabled. If the EN pin is pulled below 1.16V, that channel is disabled.

The EN pin can also be left floating. The EN pin has a 1μA pull-up current source that increases to 2μA during ramp-up. Please note that the EN pin has an ABSMAX voltage of 6V. The PMBus interface is still active when both EN pins are low which means users can program the device and readback the internal register values.

CONTROL LOOP

The ES5325 uses the output voltage information and the inductor current information to regulate the output voltage. The output voltage is differentially sensed by the FB and V_{OSNSP} pins. The sensed signal is compared with internal 0.5V reference and the voltage difference is amplified by a transconductance amplifier to the COMP pin. The COMP pin indicates the target peak inductor current. If the output voltage decreases, the ES5325 increases the target inductor peak current to raise the output voltage; if the output rises, the ES5325 decreases the target peak inductor current to reduce the output voltage.

At the beginning of each clock cycle, the high-side power MOSFET is turned on. When the inductor current reaches the peak current value set by the COMP pin, the high-side power MOSFET is turned off; the low-side power MOSFET is turned on. The high-side power MOSFET is turned on again at the beginning of next clock cycle. The Regulator regulates the output voltage by repeating this operation.

V_{INT}/V_{DRV} UVLO

The ES5325 integrates one high performance, low dropout linear 5V V_{INT} regulator, which powers most blocks. The input voltage SV_{IN} can be high up to 16V. Connect a minimum 4.7μF low ESR ceramic capacitor from the output V_{INT} to GND. When the V_{INT} voltage is lower than the UVLO falling threshold of 3.8V, the ES5325 stops switching. It resumes switching after the V_{INT} voltage is higher than 4.1V.

When the V_{DRV} voltage is lower than the UVLO falling threshold of 3.45V, the ES5325 stops switching. It resumes switching after both the V_{DRV} voltage are higher than 3.85V.

Don't apply more than 6V to the V_{DRV} pin.

START-UP

The ES5325 incorporates an external SS pin to smoothly ramp up the output to the desired voltage when the device is enabled. During start-up, an internal 1μA current source begins charging up the soft-start capacitor connected to the SS pin. The voltage error amplifier reference voltage is clamped to the voltage on the SS pin when the SS pin voltage is less than 0.5V. Therefore, the output voltage rises from 0V to regulation. The SS pin can also be used for tracking.

The soft start time can be calculated based on the function below:

$$t_{ss} = \frac{0.5V \cdot C_{ss}(\mu F)}{1\mu A}$$

When the soft-start time set by the external capacitor is less than 1ms, an internal soft-soft circuit of 1ms takes over the soft-start.

If the output is pre-biased to a certain voltage before start-up, the ES5325 disables the switching of both the high-side and low-side power MOSFETs until the voltage on the SS pin exceeds the sensed voltage by the FB and V_{OSNSN} pins.

OPERATION MODE

By default, the ES5325 operates in Continuous Conduction Mode (CCM). In CCM, low-side power MOSFET resumes switching neglecting zero load current condition.

If channel's DCM bit in the MFR_SETTNG command is set to be 1, the channel operates in DCM. In DCM, the low-side power MOSFET turns off when the load current

ramps to near zero, preventing recirculation current that can seriously reduce efficiency under light load condition.
When the SS pin is below 0.15V, the ES5325 always operates in DCM.

DIFFERENTIAL OUTPUT VOLTAGE REMOTE SENSING

The ES5325 supports differential remote output voltage sense function. The dedicated V_{OSNSN} pin helps provide the remote GND voltage sense, cooperating with remote output feedback voltage sense pin FB. Differential output voltage remote sensing allows for more accurate output regulation in high power distributed systems which have large line losses.

INITIAL OUTPUT VOLTAGE SET METHOD

The PWM controller has an internal 0.5V reference voltage. As shown in the Block Diagram, a 60.4kΩ accuracy internal feedback resistor connects from the V_{OSNSP} pin to the FB pin.
Adding a resistor R_{FB} from FB to V_{OSNSN} set the initial output voltage as following equation:

$$V_{Initial} = 0.5V \cdot \frac{60.4k\Omega + R_{FB}}{R_{FB}}$$

Table 1 FB Resistor Table vs Various Output Voltages

V_{OUT}(V)	0.5	1.0	1.2	1.5	1.8	3.3	5
R_{FB}(kΩ)	OPEN	60.4	43.2	30.1	23.2	10.7	6.65

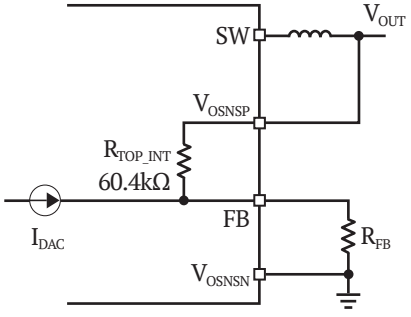


Figure 2 Output Voltage Programming Diagram

OUTPUT VOLTAGE DIGITAL PROGRAMMING

Post start-up, each channel output voltage can be digitally programmed by the user at any time with a write to PMBus VOUT_COMMAND. By writing to the VOUT_COMMAND register, the built-in programmable current DAC, which has a full range of ±64μA with a minimum adjustable step of 0.5μA, will inject or source current to or from the FB pin to adjust the output voltage on the fly. See Figure 3.

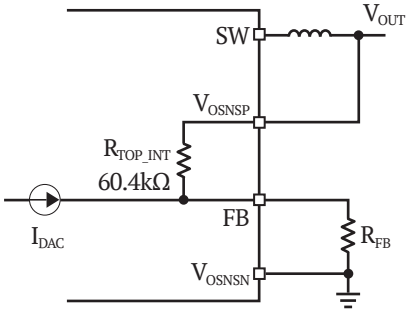


Figure 3 Output Voltage Digital Programming with Internal Top Feedback Resistor

The adjusted output voltage can be calculated as:

$$V_{OUT} = V_{Initial} - I_{DAC\_Total} \cdot R_{TOP\_INT}$$

Where the $V_{Initial}$ is the initial output voltage set by the feedback resistor R_{FB} and R_{TOP_INT}. I_{DAC} is the built-in DAC current commanded by VOUT_COMMAND, See Table 2. The R_{TOP_INT} is the built-in 60.4kΩ internal top feedback resistor between the V_{OSNSP} and FB pins. By solving the equation above, it is easy to get the LSB of output voltage adjustment is 30.2mV per step while using the built-in internal top feedback resistor.

Table 2 VOUT_COMMAND Command Setting vs I_{DAC} Current

BIT	VALUE	I_{DAC} Current
7	0 1	0 -64μA
6	0 1	0 32μA
5	0 1	0 16μA
4	0 1	0 8μA
3	0 1	0 4μA
2	0 1	0 2μA
1	0 1	0 1μA
0	0 1	0 0.5 μA

If the 30.2mV per step adjustment does not satisfy the accuracy of the specific application, per step voltage can be reduced by using an external top feedback resistor R_{TOP_EXT} in parallel with the internal R_{TOP_INT} which is 60.4kΩ. See Figure 4.

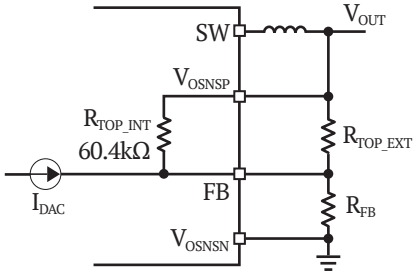


Figure 4 Output Voltage Digital Programming with External Top Feedback Resistor

By doing this, the initial output voltage can be set as:

$$V_{Initial} = 0.5V \cdot \frac{R_{TOP\_INT} // R_{TOP\_EXT} + R_{FB}}{R_{FB}}$$

And the output voltage can be digital programmed as:

$$V_{OUT} = V_{Initial} - I_{DAC\_Total} \cdot (R_{TOP\_INT} // R_{TOP\_EXT})$$

with a minimum programmable step of:

$$0.5\mu A \cdot (R_{TOP\_INT} // R_{TOP\_EXT})$$

OUTPUT VOLTAGE RAMPING

The output ramping speed can be programmed by MFR_VOUT_SLEW_RATE command. This one-byte register configs the ramping time delay by setting the switching clock cycles between the output voltage minimum adjustable steps, which is 0.5μA × R_A explained in last section. See Table 3 for MFR_VOUT_SLEW_RATE command setting vs ramping switching clock cycles. The default value for this command is 0x00.

Table 3 MFR_VOUT_SLEW_RATE command setting vs Switching Clock Cycles

[3:0]	Switching Clock	[3:0]	Switching Clock
0000	1024	1000	256
0001	2	1001	1024
0010	4	1010	2048
0011	8	1011	4096
0100	16	1100	4096
0101	32	1101	4096
0110	64	1110	4096
0111	128	1111	4096

POWER GOOD INDICATOR

The PG pin is an open drain power good indicator controlled by a windows comparator. If the regulated feedback voltage (FB-V_{OSNSN}) is within the ±10% window of 500mV reference voltage, the PG pin will be high impedance. The PG pin should be connected to V_{INT} or another voltage source through a typical 10kΩ ~100 kΩ resistor.

When the regulated feedback voltage leaves the ±10% window of 500mV reference voltage, the PG pin will be pulled low after a 60μs deglitch filter.

OVER VOLTAGE PROTECTION

The ES5325 features output over voltage protection. If the sensed feedback voltage is higher than 550mV, the low-side Power MOSFET will keep on until the sensed feedback voltage drops back to the ±10% window of 500mV reference voltage.

OVER CURRENT PROTECTION (HICCUP MODE)

The ES5325 continuously monitors the inductor current. When an overcurrent fault is detected for 64 consecutive clock cycles, the Regulator turns off both the high-side and low side power MOSFET, resets the soft-start capacitor and waits for 32768 clock cycles before attempting to start-up again.

OVER TEMPERATURE PROTECTION

When the ES5325 die temperature reaches 160°C, the switching stops and both SS pins are pulled to ground. The ES5325 goes back switching after the die temperature reduces to be less than 140°C.

TRANSIENT IMPROVEMENT OPERATION

ES5325 features a proprietary transient improvement function. When the ENFAST Bit in MFR_SETTING command is set, the load transient improvement feature is enabled. During a large step-down load transient, the ES5325 will increase the switching frequency for several clock cycles to reduce the output voltage drop.

MULTIPHASE OPERATION

For outputs requiring more than 20A load current, multiple ES5325 devices can be paralleled to provide it. Increase output current without increasing input and

output voltage ripple.

The ES5325 can be configured for single-output multiphase operation with the following connections: Connect the EN, COMP, SS, FB, SYNC pins of the parallel channel together. Program one ES5325 as a SYNC output, all other ES5325 as SYNC inputs. (SYNC INPUT has a 90° phase difference from SYNC OUTPUT) Figure 5 shows a 2-phase design.

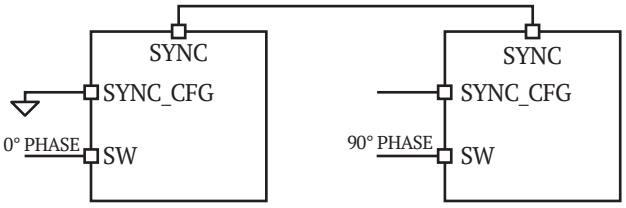


Figure 5 2-Phase Design

PMBUS INTERFACE

PMBus is a two-wire serial interface which is used for communication between ICs and systems. The bus consists of a clock line (SCL) and a data line (SDA). A PMBus master controls the bus by generating the SCL signal and controlling the data transfer. The ES5325 works as PMBus slave to support the data transfer.

PMBUS TRANSFER FORMAT

The Figure 6 shows the timing relationship of the signal of the bus.

The PMBus master transmits a START condition to begin the communication. The START signal is generated by transitioning SDA from high to low while keeping SCL high. Once the data transfer finishes, the master transmits a STOP signal to end the communication. The STOP signal is transmitted by master by pulling SDA from low to high while the SCL is high. The PMBus Write and Read command format is shown in Figure 7.

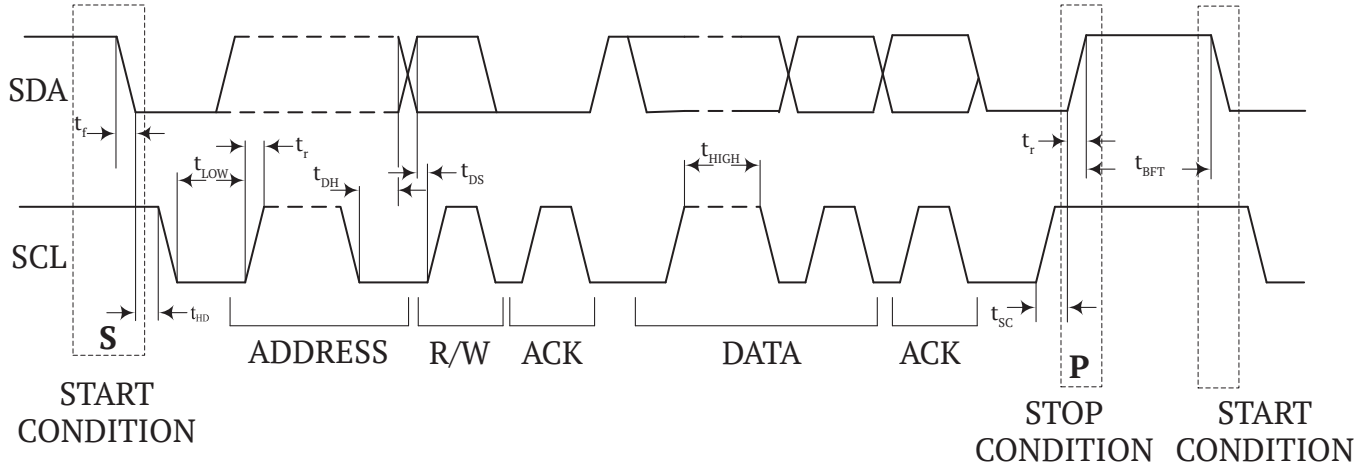


Figure 6 PMBus Timing Diagram

1	7	1	1	8	1	1
S	SLAVE ADDRESS	Wr	A	DATA BYTE	A	P
			X		X	

S Start Condition

Sr Repeated Start Condition

Rd Read(BIT VALUE = 1)

Wr Write(BIT VALUE =0)

A Acknowledge(This BIT = 0 for an ACK or 1 for a NACK)

P Stop Condition

Slave to Master

Master to Slave

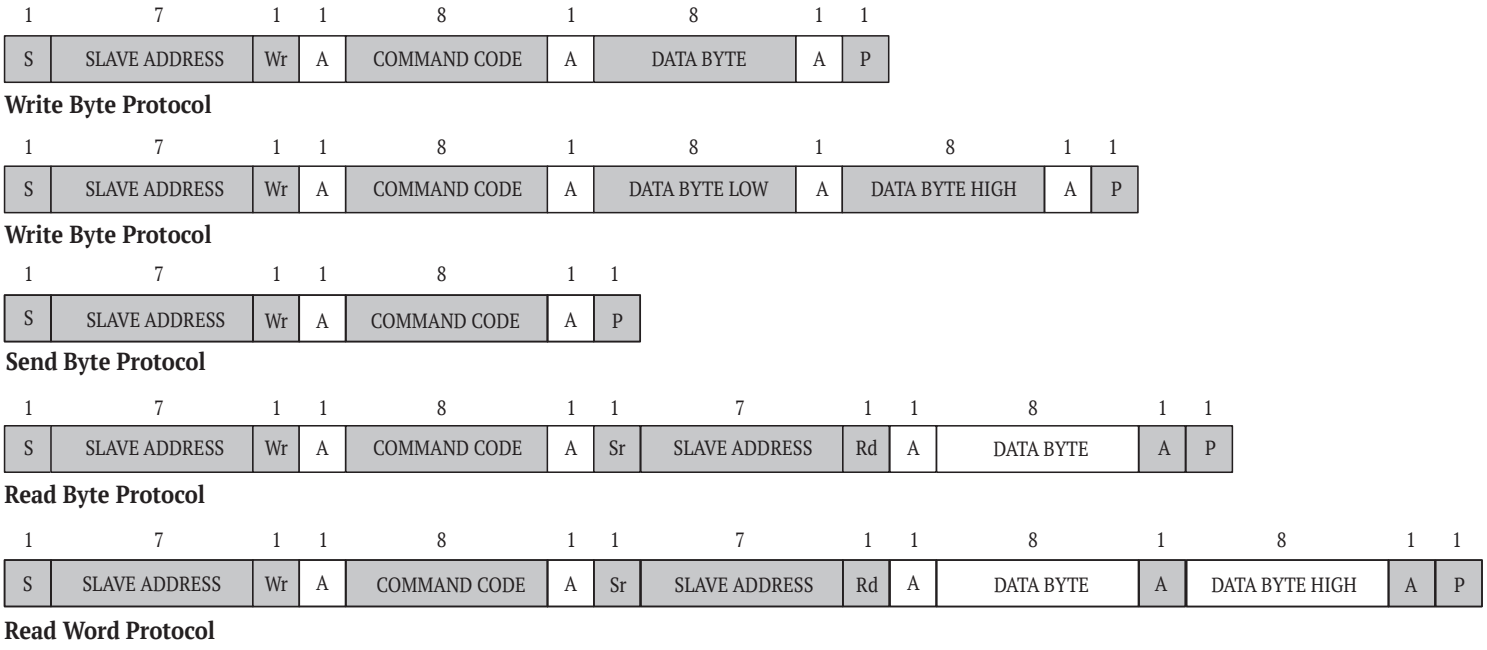


Figure 7 Write and Read Protocol

PMBUS ADDRESS

The ES5325 offers three different type PMBus addressing: global, device, and rail.

Global addressing allows the PMBus master to address all ES5325 devices on the bus. Global address cannot be disabled. There are two global address. One ES5325 global address is fixed 0x7A (7 bit). Commands sent to this global address act the same as Page is set to 0xFF. The other global address 0x7B (7 bit) is paged and allows channel specific command. Reading from global address is strongly discouraged.

Device addressing is the standard addressing method. In ES5325, the device address is set by the of the ADDR as shown in Table 4. A Device addressing is stored at MFR_ADDRESS register.

Table 4 PMBus Address Setting

Resistor (kΩ)	ADDR Pin
	Device Address
0	0000000
1.02	0000001
2.21	0000010
3.57	0000011
5.23	0000100
7.15	0000101
9.53	0000110
12.4	0000111
16.2	0001000
21.5	0001001
28.7	0001010
39.2	0001011
57.6	0001100
93.1	0001101
200	0001110
Open	0001111

Rail addressing allows the PMBus master to simultaneously communicate with all channels in multi-phase system. The rail address can be assigned with the paged MFR_RAIL_ADDRESS command. Reading from rail address is strongly discouraged.

PMBUS COMMAND DETAILS

Table 5 PMBus Command Summary

CMD CODE	COMMAND NAME	TYPE	DEFAULT	UNITS	DESCRIPTION
01h	OPERATION	R/W Byte	0x80		Turn the unit on and off in conjunction with the EN pin.
03h	CLEAR_FAULTS	Send Byte			Clear any fault bits that have been set.
20h	VOUT_MODE	R Byte	0x40		Output voltage format.
21h	VOUT_COMMAND	R/W Word	0x0000		Adjust the output voltage.
24h	VOUT_MARGIN_HIGH	R/W Word	0x0000		Adjust the output voltage.
25h	VOUT_MARGIN_LOW	R/W Word	0x0000		Adjust the output voltage.
42h	VOUT_OV_WARN_LIMIT	R/W Word	0x1388	1mV	Output overvoltage warning limit.
4Ah	IOUT_OC_WARN_LIMIT	R/W Word	0x0600	31	Output overcurrent warning limit.
51h	OT_WARN_LIMIT	R/W Word	0x0091	1°C	Output overtemperature warning limit.
57h	VIN_OV_WARN_LIMIT	R/W Word	0x1480	8mV	Input overvoltage warning limit.
78h	STATUS_BYTE	R Byte	0x00		One-byte summary of the unit's fault condition.
79h	STATUS_WORD	R Word	0x0000		Two-byte summary of the unit's fault condition.
88h	READ_VIN	R Word	0x0000	8mV	Measured V_{IN} voltage.
8Bh	READ_VOUT	R Word	0x0000	1mV	Measured V_{OUT} voltage.
8Ch	READ_IOUT	R Word	0x0000	31	Measured output current.
8Dh	READ_TEMPERATURE_1	R Word	0x0019	1°C	External sensed temperature.
8Eh	READ_TEMPERATURE_2	R Word	0x0019	1°C	Internal sensed temperature.
98h	PMBUS_REVISION	R Byte	0x33		PMBus revision supported by this device.
99h	MFR_DEVICE_ID	R Byte	0x80		Device ID.
9Ah	MFR_PIN_SETTING	R Byte			Device ILMT, RT, MODE Pins setting.
ABh	MFR_VOUT_PEAK	R Word	0x0000	1mV	Maximum measured value of READ_VOUT.
B1h	MFR_IOUT_CAL_GAIN_TC	R/W Byte			Temperature coefficient of the current sensing element.
BBh	MFR_VIN_PEAK	R Word	0x0000	8mV	Maximum measured value of READ_VIN.
BCh	MFR_IOUT_PEAK	R Word	0x0000	31	Maximum measured value of READ_IOUT.
BDh	MFR_TEMPERATURE_1_PEAK	R Word	0x0019	1°C	Maximum measured value of READ_TEMPERATURE_1.
BEh	MFR_TEMPERATURE_2_PEAK	R Word	0x0019	1°C	Maximum measured value of READ_TEMPERATURE_2.
BFh	MFR_CLEAR_PEAKS	Send Byte			Clears all peak values.
C7h	MFR_VOUT_SLEW_RATE	R/W Byte	0x00		Output voltage adjustment slew rate.
C9h	MFR_ADDRESS	R Byte			Record the PMBus address set by the ADDR pins.
CAh	MFR_RAIL_ADDRESS	R/W Byte	0x00		Set the PMBus rail address.
CBh	MFR_SETTING	R/W Byte	0x00		Adjust ES5325 Setting (DCM, ENFAST).
CCh	MFR_SMBALERT_MASK	R/W Byte	0x00		Blank signal to trigger ALERTB pin.

OPERATION (01h)

The OPERATION command is used to turn the device output on or off in conjunction with the input from the EN pins. It is also used to set the output voltage to upper or low margin voltages.

The ON bit (BIT[7]) has the same function as the EN pin. The output is on when both the ON bit and the EN pin are high. The ON bit is automatically reset to 1 after an EN pin shutdown, power cycle, or MFR_RESET command. The default value for OPERATION is 0x80. Writing an unsupported OPERATION value will generate a CML fault and the command will be ignored.

Table 6. OPERATION command Supported Value

Supported Command Value	MEANING
0x00	Immediate off
0x80	On
0xA8	Margin high
0x98	Margin low

CLEAR_FAULTS (03h)

The CLEAR_FAULTS command is used to clear any fault bits that have been set in the STATUS_BYTE and STATUS_WORD Registers. At the same time, the ES5325 releases its ALERTB pin if it is asserted. If the fault is still present when the bit is cleared, the fault bit will remain set and the host notified by asserting the ALERTB pin low.

CLEAR_FAULTS is a paged command. This write-only command has no data bytes. Issuing a CLEAR_FAULTS command will not cause the device to restart in the event of a fault turn-off.

VOUT_MODE (20h)

The VOUT_MODE command reads and commands the output voltage. The 3 MSBs determine the data format (only direct format is supported in ES5325), and the other 5 bits represent the exponent used in the output voltage read/write commands. The default value of VOUT_MODE is 0x40. The VOUT_MODE is a Read Only command. If a host sends a VOUT_MODE write command, the ES5325 rejects the VOUT_MODE command, declare a communication fault (CML) for invalid data.

VOUT_COMMAND (21h)

Command						VOUT_COMMAND										
Format						Direct										
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Function	X					$R_A \cdot 0.5\mu A/LSB$										

Where R_A is the resistor between the FB pin and V_{OUT}.

The VOUT_COMMAND controls a current DAC value used to adjust the output. The current is injected to the FB pin. The 8 LSB byte is formatted as an 8-bit 2's complement value. Setting BIT[7] to 0 sourcing the current from the IC and BIT[7] to 1 sinks the current to the IC. The bit value and output adjustment are listed below. The default value for this command is 0x0000.

BIT	VALUE	Function
7	0 1	0 $-64\mu A \cdot R_A$
6	0 1	0 $32\mu A \cdot R_A$
5	0 1	0 $16\mu A \cdot R_A$
4	0 1	0 $8\mu A \cdot R_A$
3	0 1	0 $4\mu A \cdot R_A$
2	0 1	0 $2\mu A \cdot R_A$
1	0 1	0 $1\mu A \cdot R_A$
0	0 1	0 $0.5\mu A \cdot R_A$

VOUT_MARGIN_HIGH (24h)

The VOUT_MARGIN_HIGH has the same contents as the VOUT_COMMAND. When OPERATION=0xA8, the VOUT_MARGIN_HIGH command controls the current DAC instead of VOUT_COMMAND. The default value for this command is 0x0000.

VOUT_MARGIN_LOW (25h)

The VOUT_MARGIN_LOW has the same contents as the VOUT_COMMAND. When OPERATION=0x98, the VOUT_MARGIN_LOW command controls the current DAC instead of VOUT_COMMAND. The default value for this command is 0x0000.

VOUT_OV_WARN_LIMIT (42h)

The VOUT_OV_WARN_LIMIT command sets the value of the output voltage measured by the ADC that causes an output overvoltage warning. The READ_VOUT value will be used to determine if this limit has been exceeded. If the sensed voltage exceeds this value, the VOUT bit is set in STATUS_WORD command, and the ALERTB signal is asserted. This command has two data bytes and is formatted as unsigned binary. The default value for this command is 0x1388 which is 6V.

Command						VOUT_OV_WARN_LIMIT										
Format						Unsigned binary										
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	1	0	0	1	1	1	0	0	0	1	0	0	0
Function	x		1mV/LSB													

IOUT_OC_WARN_LIMIT (4Ah)

The IOUT_OC_WARN_LIMIT command sets the value of the output current measured by the ADC that causes an output overcurrent warning. The READ_IOUT value will be used to determine if this limit has been exceeded. If the sensed current exceeds this value, the IOUT bit is set in STATUS_WORD command, and the ALERTB signal is asserted. This command has two data bytes and is formatted as unsigned binary. The default value for this command is 0x0600 which is 96A.

Command						IOUT_OC_WARN_LIMIT										
Format						Unsigned binary										
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0
Function	X		31mA/LSB													

OT_WARN_LIMIT (51h)

The OT_WARN_LIMIT command sets the threshold for external temperature measured by the TSNS pin. If the sensed temperature exceeds this value, the OT warning bit is set in STATUS_BYTE, and the ALERTB signal is asserted. The READ_TEMPERATURE_1 value is used to determine if the limit has been exceeded. This command has two data bytes and is formatted as unsigned binary. The default value for this command is 0x0091 which is 145°C.

Command						OT_WARN_LIMIT										
Format						Unsigned binary										
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	1
Function	X					1°C/LSB										

VIN_OV_WARN_LIMIT (57h)

The VIN_OV_WARN_LIMIT command sets the value of the input voltage measured by the ADC that causes an input overvoltage warning. The READ_VIN value will be used to determine if this limit has been exceeded. If the sensed voltage exceeds this value, the VIN Bit is set in STATUS_WORD, and the ALERTB signal is asserted. This command has two data bytes and is formatted as unsigned binary. The default value for this command is 0x1480 which is 42V.

Command						VIN_OV_WARN_LIMIT										
Format						Unsigned binary										
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Default	0	0	0	1	0	1	0	0	1	0	0	0	0	0	1	0
Function	x		8mV/LSB													

STATUS_BYTE (78h)

The STATUS_BYTE command returns one byte of information with a summary of the most critical faults. The STATUS_BYTE is a paged register.

BIT	BIT NAME	BEHAVIOR	DESCRIPTION
7	RESERVED		Always read as 0.
6	OFF	Live	This bit is set if the channel is off, regardless of the reason, including simply the EN pin is low.
5:3	RESERVED		Always read as 0.
2	OT	Live	A temperature fault or warning has occurred.
1	CML	Latched	A communication fault has occurred.
0	NONE_OF_THE_ABOVE	Live	Always read as 0.

STATUS_WORD (79h)

The STATUS_WORD command returns two-byte of information with a summary of the most critical channel's fault condition. The low byte of the STATUS_WORD is the same as the STATUS_BYTE command. The

STATUS_WORD is a paged command.

BIT	BIT NAME	BEHAVIOR	DESCRIPTION
15	VOUT	Live	An output voltage fault or warning has occurred.
14	IOUT	Live	An output current fault or warning has occurred.
13	VIN	Live	An input voltage fault or warning has occurred.
12	RESERVED		Always read as 0.
11	PGOODB	Live	The Power Good state is false if this bit is set.
10:8	RESERVED		Always read as 0.

READ_VIN (88h)

The READ_VIN command returns two bytes of data in the direct data format that represent the input voltage. It is formatted as a 14-bit unsigned binary integer scaled 8mV/ bit. READ_VIN is not a paged register. The READ_VIN is read only command and the default value is 0x0000.

Command	READ_VIN
Format	Direct
LSB	8mV
Default	0x0000

READ_VOUT (8Bh)

The READ_VOUT command returns two bytes of data in the direct data format that represent the output voltage measured between the V_{OSNSN} and V_{OSNSP} pins. It is for matted as a 14-bit unsigned binary integer scaled 1mV/ bit. READ_VOUT is a paged register. PAGE register cannot be set to 0x11 for READ_VOUT command. The READ_VOUT is read only command and the default value is 0x0000.

Command	READ_VOUT
Format	Direct
LSB	1mV
Default	0x0000

READ_IOUT (8Ch)

The READ_IOUT command returns the 14-bit measured value of the output current. The reading from the Measurement System must be manipulated in order to convert the measured value into the desired value (IOUT). READ_IOUT is a paged command.

Command						READ_IOUT										
Format						Direct, 2's complement										
Default						0x0000										
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Function	X					31/LSB										

READ_TEMPERATURE_1 (8Dh)

The READ_TEMPERATURE_1 command returns 10-bit external sensed temperature, in degrees Celsius. READ_TEMPERATURE_1 is a paged command. The default value is 0x0019.

Command						READ_ TEMPERATURE_1										
Format						Direct, 2's complement										
Default						25°C (0x0019)										
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Function	X					1°C/LSB										

READ_TEMPERATURE_2 (8Eh)

The READ_TEMPERATURE_2 command returns 10-bit ES5325 internal sensed temperature, in degrees Celsius. READ_ TEMPERATURE_2 is not a paged command. The default value is 0x0019.

Command						READ_ TEMPERATURE_2										
Format						Direct, 2's complement										
Default						25°C (0x0019)										
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Function	X					1°C/LSB										

PMBUS_REVISION (98h)

The PMBUS_REVISION command returns the protocol revision used. Accesses to this command should use the read byte protocol. Bit [7:4] indicates the PMBus revision of specification Part I to which the device is compliant. Bit [3:0] indicates the revision of specification Part II to which the device is compliant.

Bit [7:4] is always read as 4'b0011, specification PMBus Part I Revision 1.3.

Bit [3:0] is always read as 4'b0011, specification PMBus Part II Revision 1.3.

MFR_DEVICE_ID (99h)

The MFR_DEVICE_ID command report the device ID which is 0x88 for ES5325. This read only commands has one data byte. It is not a paged command.

MFR_PIN_SETTING (9Ah)

The MFR_PIN_SETTING command reports the ILMT, RT pin setting. It is not a paged command. This read only commands has one data byte.

BIT	VALUE	MEANING
7	1	EN1 pin is logic high
6	1	EN0 pin is logic high
5	1	Channel 1 is in forced DCM mode
4	1	Channel 0 is in forced DCM mode
3	1	SYNC pin is programmed as SYNC IN
2:0	000	ILMT pin sets VCSMAX to 24mV
	001	ILMT pin set VCSMAX to 12mV
	010	ILMT pin set VCSMAX to 36mV
	011	ILMT pin set VCSMAX to 48mV
	100	ILMT pin set VCSMAX to 60mV

MFR_IOUT_CAL_GAIN_TC(B1h)

The MFR_IOUT_CAL_GAIN_TC command allows the user to program the temperature coefficient of the IOUT_CAL_GAIN sense resistor or inductor DCR in ppm/°C. It is a paged command. This command has one data byte. The IOUT_CAL_GAIN is multiplied by [1.0 + MFR_IOUT_CAL_GAIN_TC • (READ_TEMPERATURE_1-25)].

DCR sensing will have a typical value of 3900ppm/°C (0.0039/°C, 0x27). The valid range of the command is between 0x24(0.0036/°C) and 0x2B(0.0043/°C). If a host sends a value out of this range, the ES5325 rejects the command. It is not a paged command.

Command	MFR_IOUT_CAL_GAIN_TC							
Format	Direct, unsigned							
Default	0x27							
Bit	7	6	5	4	3	2	1	0
Function	X		0.0001°C / LSB					

MFR_VIN_PEAK(BBh)

The MFR_VIN_PEAK command reports the highest volt age, in volts, reported by the READ_VIN measurement. To clear the peak value and restart the peak monitor, use the MFR_CLEAR_PEAKS command. This command has two data bytes and is formatted as a 14-bit unsigned binary integer scaled 8mV/ bit. The MFR_VIN_PEAK is not a paged command.

MFR_VOUT_PEAK (ABh)

The MFR_VOUT_PEAK command reports the highest voltage, in volts, reported by the READ_VOUT measurement. To clear the peak value and restart the peak monitor, use the MFR_CLEAR_PEAKS command. This command has two data bytes and is formatted as a 14-bit unsigned binary integer scaled 1mV/ bit. The MFR_VOUT_PEAK is a paged command.

MFR_IOUT_PEAK (BCh)

The MFR_IOUT_PEAK command reports the highest current, in amperes, reported by the READ_IOUT measurement. To clear the peak value and restart the peak monitor, use the MFR_CLEAR_PEAKS command. This command has two data bytes and is formatted as a 14-bit 2's complement value scaled 31/bit. The MFR_IOUT_PEAK is a paged command.

MFR_TEMPERATURE_1_PEAK (BDh)

The MFR_TEMPERATURE_1_PEAK command reports the highest temperature, in degrees Celsius, reported by the READ_TEMPERATURE_1 measurement. Its LSB is 1°C. This command is cleared using the MFR_CLEAR_PEAKS command. It is a paged command.

MFR_TEMPERATURE_2_PEAK (BEh)

The MFR_TEMPERATURE_2_PEAK command reports the highest temperature, in degrees Celsius, reported by the READ_TEMPERATURE_2 measurement. Its LSB is 1°C. This command is cleared using the MFR_CLEAR_PEAKS command. It is not a paged command.

MFR_CLEAR_PEAKS (BFh)

The MFR_CLEAR_PEAKS command clears the MFR_*_PEAK data values and restarts the peak monitor routine. This write-only command requires no data bytes but will accept and ignore up to two bytes. It is not a paged command.

MFR_VOUT_SLEW_RATE (C7h)

The MFR_VOUT_SLEW_RATE controls the slew rate of current DAC which is used to offset the output. This one-byte command has four valid bits which is shown as below. The default value for this command is 0x00. MFR_VOUT_SLEW_RATE is a paged command.

[3:0]	Switching Clock	[3:0]	Switching Clock
0000	1024	1000	256
0001	2	1001	1024
0010	4	1010	2048
0011	8	1011	4096
0100	16	1100	4096
0101	32	1101	4096
0110	64	1110	4096
0111	128	1111	4096

MFR_ADDRESS (C9h)

The MFR_ADDRESS command reports the 7-bit PMBus address set by the ADDR1 and ADDR0 pins.

MFR_RAIL_ADDRESS (CAh)

The MFR_RAIL_ADDRESS command enables direct device address access to the PAGE activated channel. The value of this command should be common to all devices attached to a single power supply rail. Users should only perform command writes to this address. The MSB (BIT [7]) must be set high to enable communication using the MFR_RAIL_ADDRESS address. Setting this command to a value of 0x00 disables rail device addressing for the channel. It is a paged command.

This command has one data byte. Its default value is 0x00.

BIT	VALUE	MEANING
7	1	Enable the MFR_RAIL_ADDRESS
	0	Disable the MFR_RAIL_ADDRESS
6:0		7-Bit MFR_RAIL_ADDRESS address

MFR_SETTING (CBh)

One-byte setting command to set the ES5325 operation condition.

BIT	VALUE	MEANING
7:5		Reserved
4	1	Double the ADC Sampling Rate
3	1	Enable Method B Transient Improvement Circuit
2	1	Enable Method A Transient Improvement Circuit
1	1	Program Page1 to DCM
0	1	Program Page0 to DCM

MFR_SMBALERT_MASK (CEh)

This command provides a means by which the user can mask the ALERTB signal.

BIT	VALUE	MEANING
7:1		Reserved
0	1	Mask the CML to the ALERTB pin

MFR_RESET (CFh)

This command provides a means by which the user can perform a reset of the ES5325 PMBus interface and ADC. Write to this command to reset PMBus interface and ADC to power-on state. Write data is ignored.

DESIGN EXAMPLE

GENERAL FEATURES

Figure 8 shows an ES5325 typical design. The typical input voltage is 12V, output is 5V and output current is 20A.

The output is set by:

$$V_{OUT} = 0.5V \cdot \frac{60.4k\Omega + R_{FB}}{R_{FB}} = 0.5V \cdot \frac{60.4k\Omega + 6.65k\Omega}{6.65k\Omega} \approx 5V$$

For peak current mode control application, the typical inductor current ripple is between 30% and 50% of the maximum output current. The inductor value can be calculated if 50% is chosen as:

$$L = \frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{V_{IN} \cdot F_S \cdot 0.5 \cdot I_{OUT}}$$

$$= \frac{5V \cdot (12V - 5V)}{12V \cdot 600kHz \cdot 0.5 \cdot 20A}$$

$$\approx 490nH$$

Recommended choose 470nH (0.67mΩ DCR) Wurth 744355147.

A 4.7μF capacitor is connected to the V_{INT} pin to stabilize the V_{INT} output. SS pin has 0.1μF capacitor for external soft-start purpose. There is 0.1μF capacitor between BOOST and PHASE pins to store the energy to turn on the top Power MOSFET.

TYPICAL APPLICATIONS

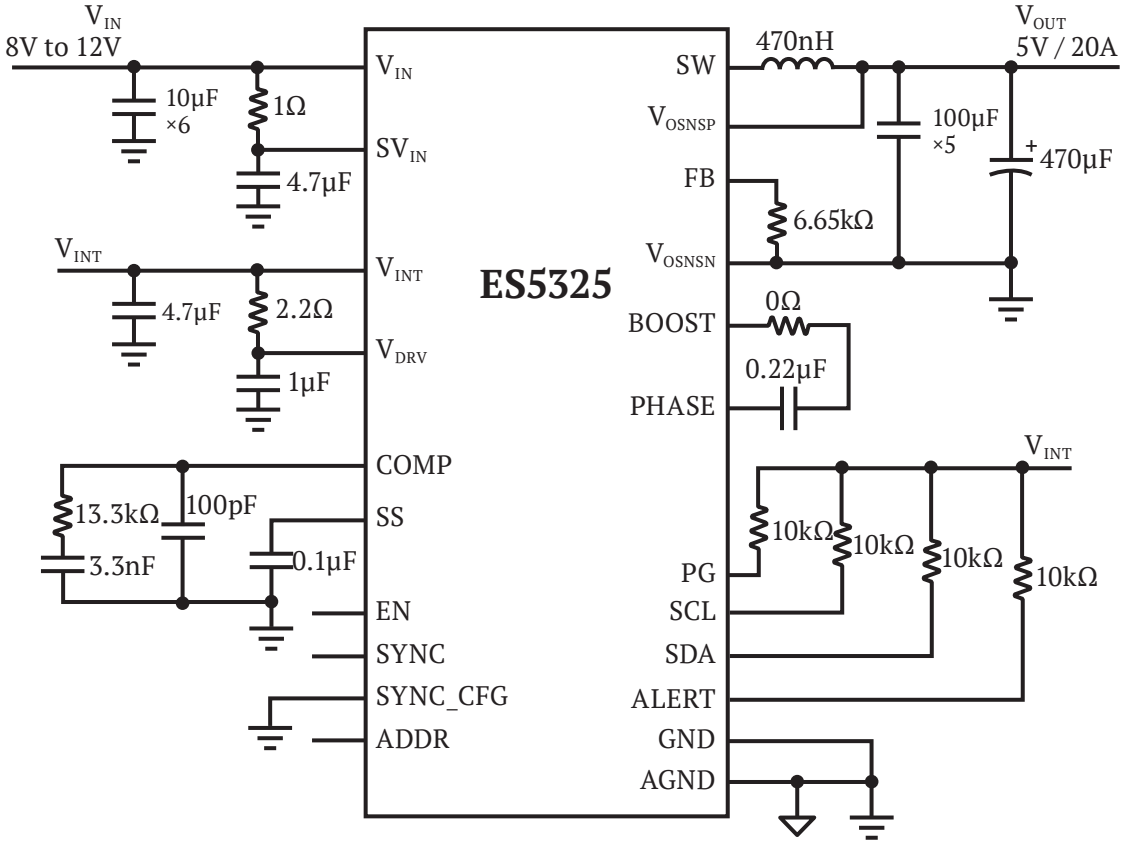


Figure 8 Typical 8V to 12V Input, 5V at 20A Output Design

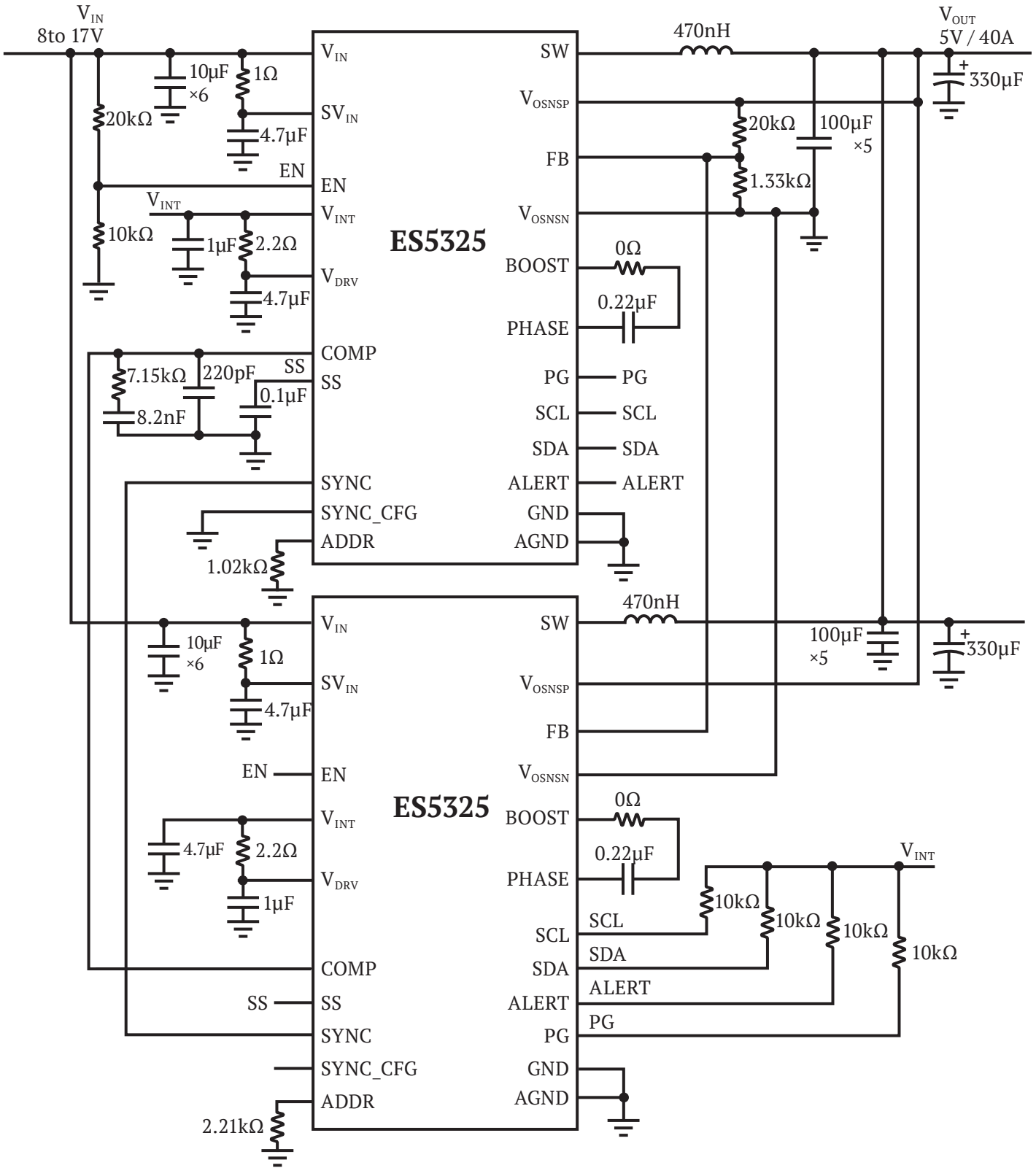


Figure 9 8V to 17V Intermediate Bus Input, 2-Phase Parallel 5V Output at 40A Design

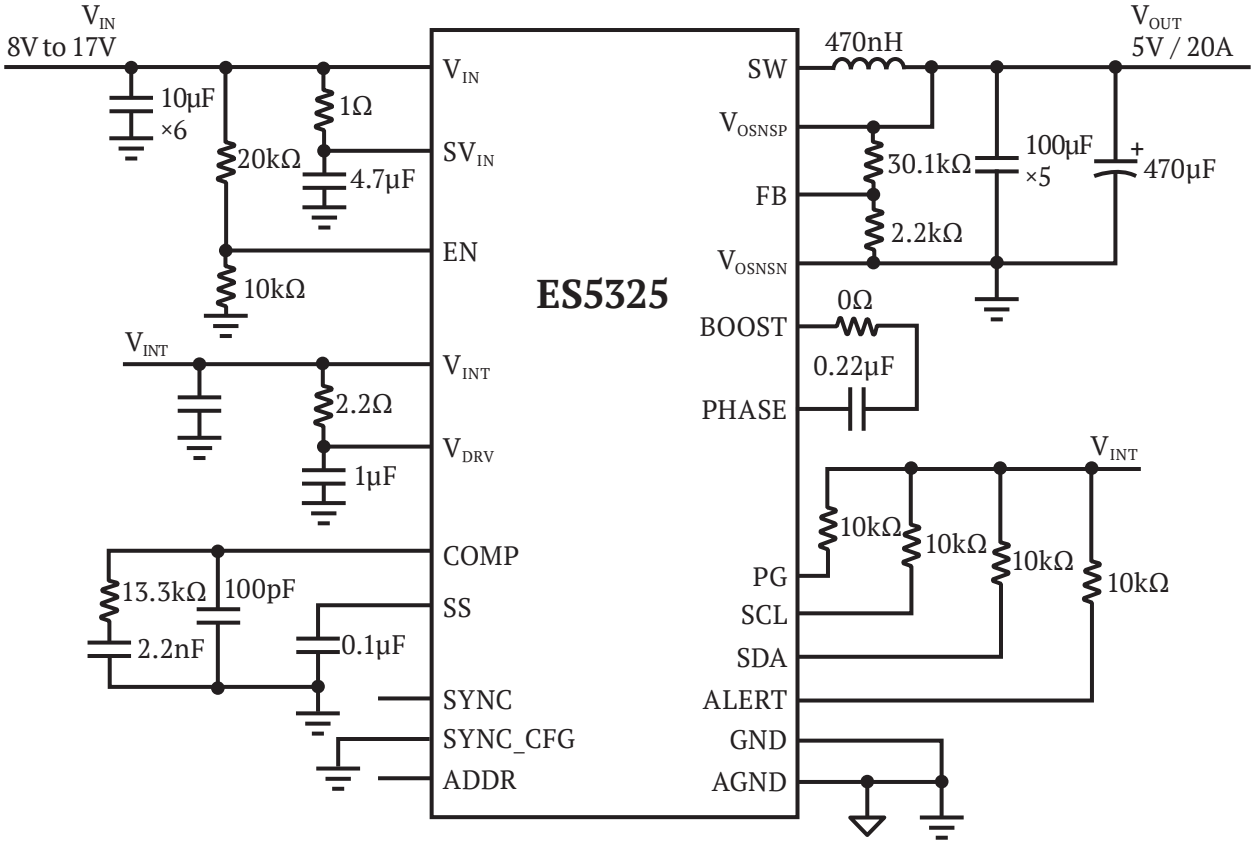
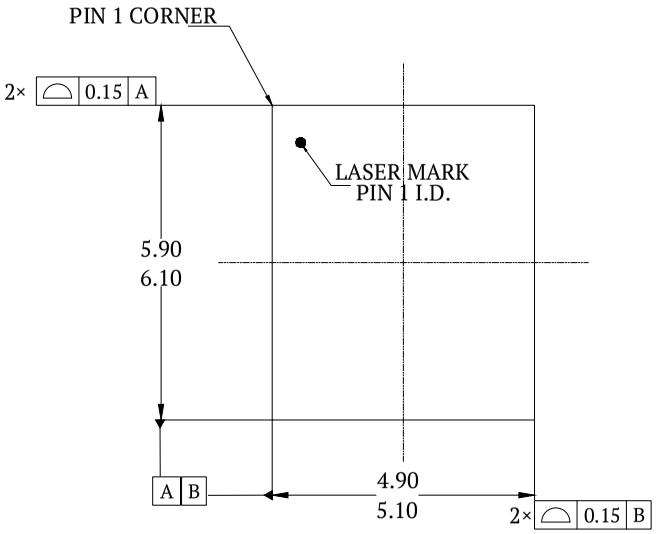
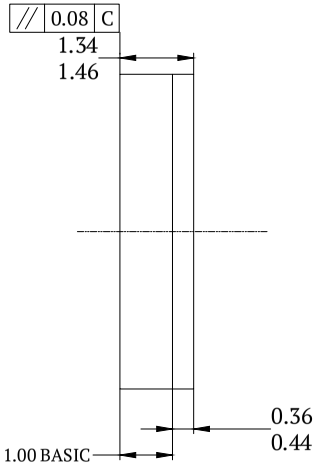


Figure 10 8V to 17V Input, 5V Output 10mV Pressure Regulatic Design

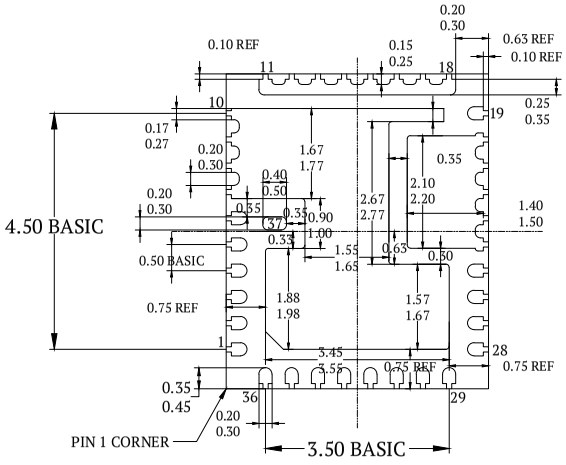
LQFN PACKAGE
37-LEAD 5.00mm × 6.00mm × 1.40mm
POD-0032-A2
Unit: mm



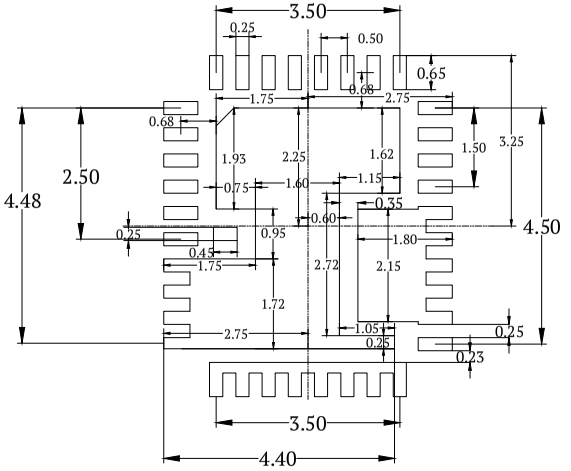
TOP VIEW



SIDE VIEW

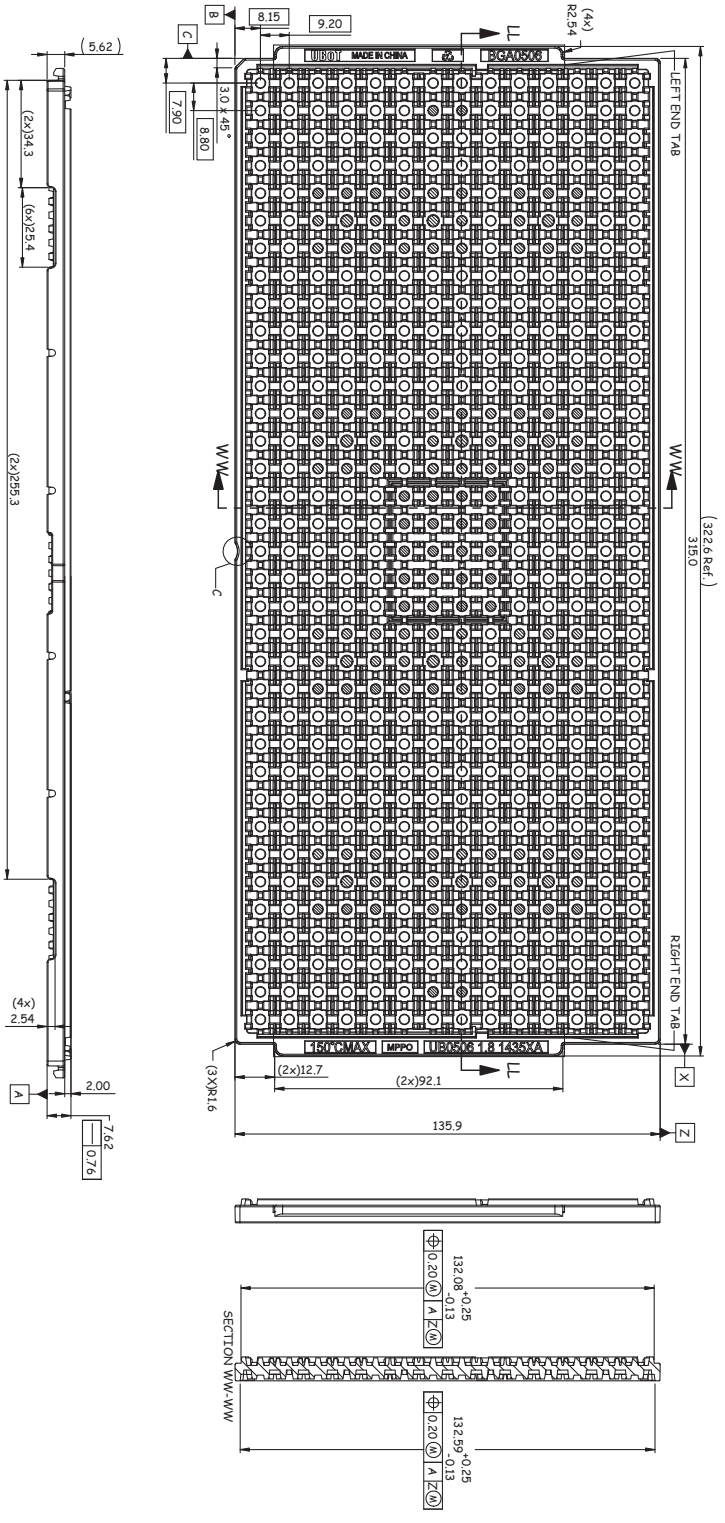


BOTTOM VIEW



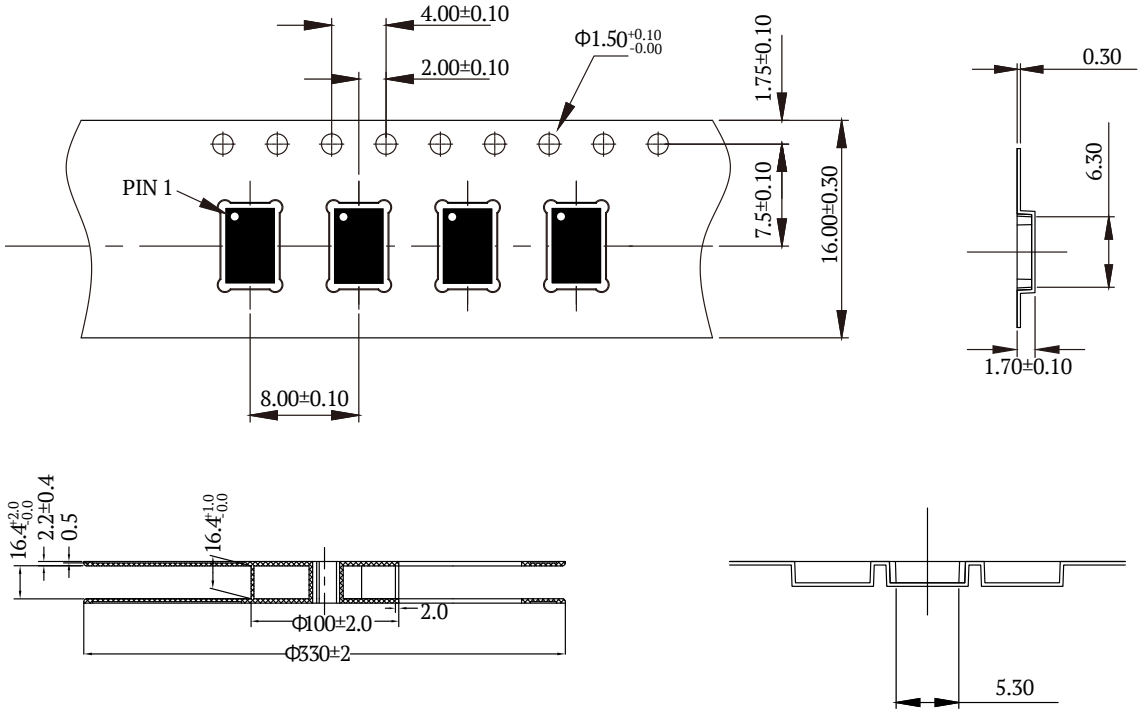
SUGGESTED PCB LAYOUT TOP VIEW

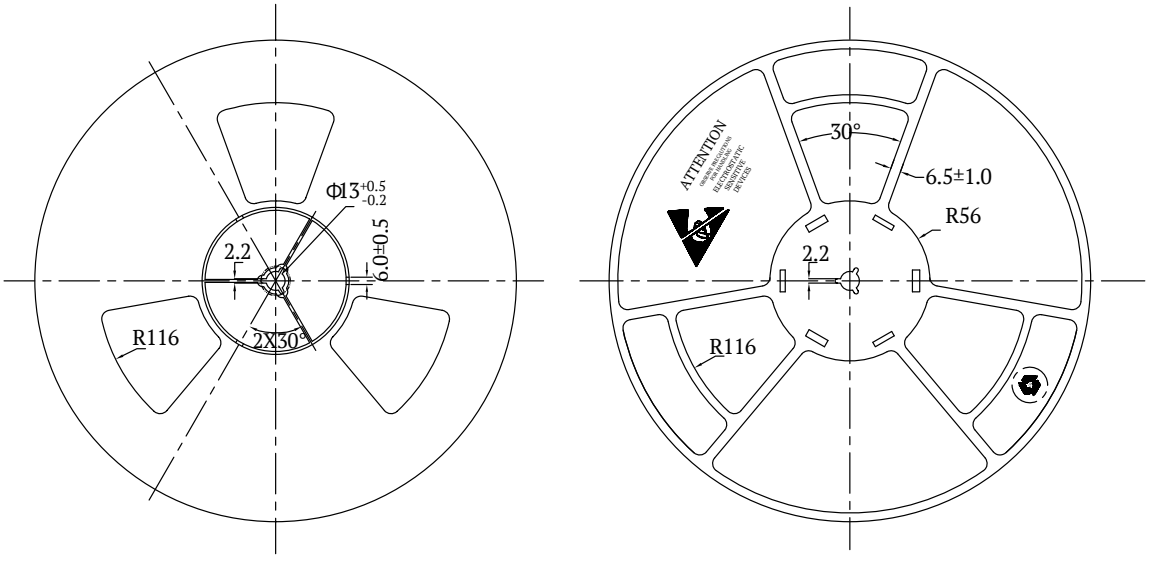
PACKAGE MATERIAL (TRAY)



PART NO.	PMT 0030
TRAY TYPE	5×6×1.45mm
QTY	490ea/Pcs
UNIT SIZE	mm

PACKING MATERIAL (TAPE&REEL)





NOTE:

1. Unit Size: mm
2. SPQ: 3000 PCS