3.2V to 65V Input, 8A Synchronous Step-Down Converter with 3µA Quiescent Current

DESCRIPTION

The ES5608/ES5609 is a monolithic synchronous step-down DC/DC converter capable of providing up to 8A current from a 3.2V to 65V input supply. It features low noise architecture designed to minimize EMI emissions while delivering high efficiency at high switching frequencies. This includes the integration of bypass capacitors to optimize all the fast current loops inside and makes it easy to achieve advertised EMI performance with reduced layout sensitivity.

The clean, low overshoot switching edges enable high efficiency operation even at high switching frequencies, leading to a small overall solution size. Peak current mode control with 25ns minimum on-time allow high step-down ration even at high switching frequency. The ES5609 uses external compensation to enable current sharing and fast transient response at high switching frequencies. Auto-sleep mode operation enables low standby current consumption or spread spectrum operation can further reduce EMI emissions. Soft-start and tracking functionality is accessed via the TK/SS pin and an accurate input voltage UVLO threshold can be set using the EN/UV pin.

APPLICATIONS

- Industrial Supplies and Automotive
- Low EMI and Low Noise Step-Down

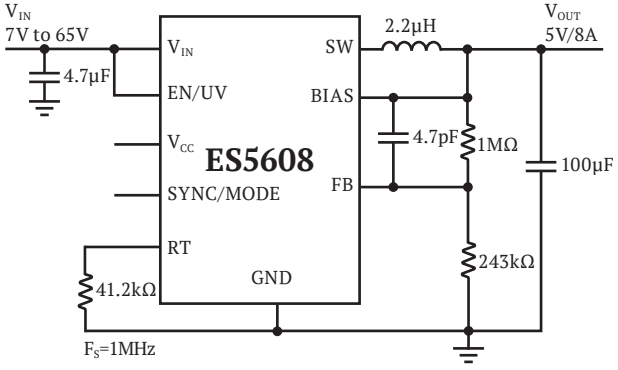
FEATURES

- **Second Generation ExSilent® Technology**
  - **Ultralow EMI Emissions on Any PCB**
  - **Eliminates PCB Layout Sensitivity**
  - **Internal Bypass Capacitors Reduce Radiated EMI**
  - **Optional Spread Spectrum Modulation**
  - **No Switching Ringing**
- Input Voltage Range: 3.2V to 65V
- 8A Continuous Output Current
- Up to 93.5% Efficiency at 1MHz, $12V_{IN}$ to $5V_{OUT}$
- Up to 91% Efficiency at 2MHz, $12V_{IN}$ to $5V_{OUT}$
- Peak Current Mode Control
- Low Quiescent Current Auto-Sleep Mode Operation
- ES5608 with 3µA Iq Regulating $12V_{IN}$ to $5V_{OUT}$
- Low Dropout Under All Conditions: 60mV at 1A
- Minimum On Time = 25ns, Capable of Very Low Duty Cycles
- ES5609 with External Compensation: Fast Transient Response and Current Sharing
- Adjustable and Synchronizable: 200kHz to 2.2MHz
- Output Soft-Start and Power Good
- Safely Tolerates High Reverse Current
- Available in 32-Lead 4mm × 6mm LQFN Package
- Please Refer to the ES5608-AEC for the Automotive Grade Version.

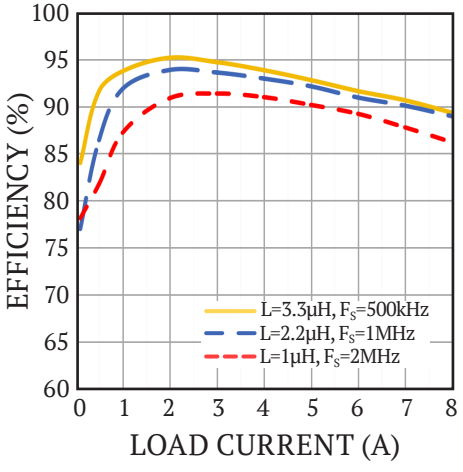
PART NUMBER	INTERNAL CAPS	COMPENSATION
ES5608	Yes	Internal
ES5609	Yes	External

TYPICAL APPLICATION

7V to 65V Input, 5V Output DC/DC Regulator

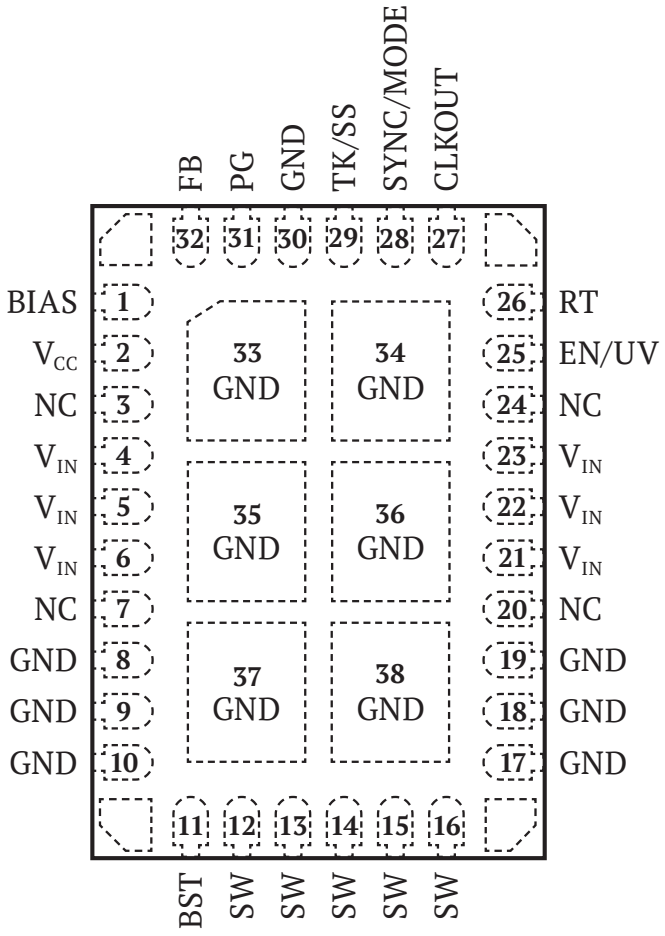


$12V_{IN}$ to $5V_{OUT}$ EFFICIENCY

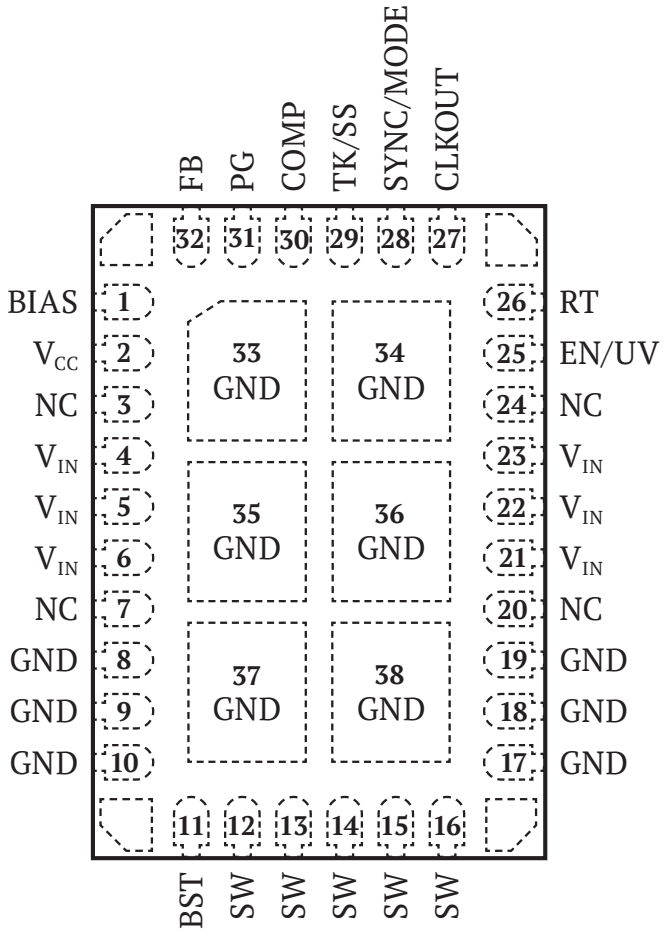


PIN CONFIGURATION AND FUNCTIONS

ES5608 (TOP VIEW)



ES5609 (TOP VIEW)



32-LEAD 4mm × 6mm × 0.97mm LQFN Package

θ_{JCTOP} = 3.3°C/W, θ_{JCBOT} = 4.5°C/W, θ_{JA} = 15.8°C/W, θ_{JB} = 5.7°C/W

PIN#	PIN Name	PIN Description
1	BIAS	External BIAS Supply Pin. The internal regulator will draw current from BIAS instead of V_{IN} when BIAS is tied to a voltage higher than 3.1V. For output voltages of 3.3V to 22V this pin should be tied to V_{OUT}. If this pin is tied to a supply other than V_{OUT}, use an 1μF local bypass capacitor on this pin. If no supply is available, tie to GND. However, especially for high input or high frequency applications, BIAS should be tied to output or an external supply of 3.3V or above.
2	V_{CC}	Internal 3.4V Regulator Bypass Pin. The internal power drivers and control circuits are powered from this voltage. Do not load the V_{CC} pin with external circuitry. V_{CC} current will be supplied from BIAS if BIAS > 3.1V, otherwise current will be drawn from V_{IN}. Voltage on V_{CC} will vary between 2.8V and 3.4V when BIAS is between 3.0V and 3.6V.
3, 7, 20, 24	NC	No Connect. These pins are not connected to any internal circuitry.

PIN#	PIN Name	PIN Description
4-6, 21-23	V_{IN}	The V_{IN} pins supply current to the ES5608/ES5609 internal circuitry and to the internal topside power switch. These pins must be tied together and be locally bypassed with a capacitor of 4.7µF or more. Be sure to place the positive terminal of the input capacitor as close as possible to the V_{IN} pins, and the negative capacitor terminal as close as possible to the GND pins.
8-10, 17-19, 33-38	GND	Ground Pins.
11	BST	Boot-Strap Pin. Supply high side MOSFET gate driver. This pin should be floated.
12-16	SW	Switch Pins. Connect these pins to the switching node of inductor.
25	EN/UV	Device Enable Pin. To enable the device, this pin needs to be pulled higher than 1.03V. Tying it below 0.97V places the device into shutdown.
26	RT	Frequency Set Pin. Connect an external resistor from this pin to ground to program the switching frequency from 200kHz to 2.2MHz.
27	CLKOUT	Clock Output Pin. In spread spectrum and synchronization modes, the CLKOUT pin provides a 50% duty cycle square wave 180 degrees out of phase with the switching frequency. The low and high levels of the CLKOUT pin are ground and V_{CC} respectively, and the drive strength of the CLKOUT pin is several hundred ohms. In Auto-sleep mode operation, the CLKOUT pin will be low. Float this pin if the CLKOUT function is not used.
28	SYNC/ MODE	External Synchronization and Mode Select Pin. Tie this pin to ground to enable high efficiency Auto-sleep mode operation at light load. Leave the pin floating to select Discontinuous Conduction Mode (DCM). Tie to V_{CC} to select DCM with low EMI spread spectrum modulation. Drive this pin with an external clock to synchronize the ES5608/ ES5609 switching and DCM is selected.
29	TK/SS	Output Tracking and Soft-Start Input Pin. Force a voltage below 0.97V on this pin to bypass the internal reference input to the error amplifier. Above 0.97V, the tracking functions stops and the internal reference resumes control of the error amplifier. An internal 2µA pull-up current allows to use an external capacitor to program the output voltage slew rate. This pin will be pulled to ground during fault and shutdown conditions.
30	GND (ES5608)	Ground Pin. Connect this pin to the system ground and ground plate. This pin can be left floating on PCB to be pin compatible with the ES5609.
	COMP (ES5609)	Error Amplifier Compensation Pin. The COMP pin is the output of the internal error amplifier. The voltage on this pin controls the peak inductor current. Tie an RC network from this pin to ground to compensate the control loop.
31	PG	Power Good Indicator. The open drain output is pulled high by external resistor when the FB pin voltage is within ±8% of regulation point.
32	FB	Error Amplifier Feedback Pin. Connect this pin to the external resistor divider network to program the desired output voltage. Also, connect a phase lead capacitor between FB and V_{OUT}. Typically, this capacitor is 1pF to 100pF.

ORDER INFORMATION

PART NUMBER	FINISH	MARKING	PACKAGE TYPE	PACKING MATERIAL	MSL	TEMPERATURE RANGE
ES5608IW#PBF	Au(RoHS)	5608	LQFN	TRAY	3	-40°C to 125°C
ES5608IW#TRPBF	Au(RoHS)	5608	LQFN	TAPE & REEL	3	-40°C to 125°C
ES5609IW#PBF	Au(RoHS)	5609	LQFN	TRAY	3	-40°C to 125°C
ES5609IW#TRPBF	Au(RoHS)	5609	LQFN	TAPE & REEL	3	-40°C to 125°C

ABSOLUTE MAXIMUM RATINGS

	MIN	TYP	MAX	UNIT
Terminal Voltage				
V_{IN}, EN/UV	-0.3		68	V
PG	-0.3		42	V
BIAS	-0.3		25	V
SYNC/MODE, CLKOUT, V_{CC}	-0.3		6	V
FB, TK/SS	-0.3		4	V
SW (DC)	-0.3		V_{IN}+0.3	V
SW (AC, less than 10ns)	-5		V_{IN}+5	V
BST-SW	-0.3		6	V
Temperatures				
Internal Operating Temperature Range	-40		125	°C
Storage Temperature Range	-65		150	°C
Peak Solder Reflow Package Body Temperature		260		°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

ESD RATINGS

	VALUE	UNIT
HBM (Human Body Model)	2	kV
CDM (Charged Device Model)	1	kV

Note: JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process. JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

RECOMMENDED OPERATING CONDITIONS

	MIN	TYP	MAX	UNIT
Supply Input Voltage	3.2		65	V
Output Voltage	0.97			V
Output Current			8	A
Power Good Pull-Up Voltage			40	V

Note: The device is not guaranteed to function outside its operating conditions.
Note: The ES5608/ES5609 includes overtemperature protection. The overemperature protection is active when the die temperature reaches 160°C. Continuous operation above the recommended maximum operation junction temperature may impair device reliability.

ELECTRICAL CHARACTERISTICS

The Y denotes the specifications which apply over the Full Temperature Range (FTR) (Note 2). Typical values are at T_J = 25°C. V_{IN} = 24V, V_{EN} = 24V unless otherwise specified. The values are guaranteed by test, design, or statistical correlation.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	FTR
INPUT AND ENABLE							
Minimum Input Voltage	V_{IN}			3.2	3.4	V	Y
Shutdown Current	I_{SHDN}	$V_{EN/UV}$ = 0V		2.4	5	μA	
ES5608 V_{IN} Quiescent Current in Sleep (Internal Compensation)	I_{Q_ES5608}	$V_{EN/UV}$ = 2V, V_{FB} > 0.97V, $V_{SYNC/MODE}$ = 0V, V_{BIAS} = 0V		3	10	μA	
ES5609 V_{IN} Quiescent Current in Sleep (External Compensation)	I_{Q_ES5609}	$V_{EN/UV}$ = 2V, V_{FB} > 0.97V, $V_{SYNC/MODE}$ = 0V, V_{BIAS} = 0V		140		μA	
ES5609 BIAS Quiescent Current in Sleep	I_{BIAS}	$V_{EN/UV}$ = 2V, V_{FB} > 0.97V, $V_{SYNC/MODE}$ = 0V, V_{BIAS} = 5V		200		μA	
ES5608 V_{IN} Quiescent when Active		$V_{EN/UV}$ = 2V, V_{FB} > 0.97V, $V_{SYNC/MODE}$ = 2V, V_{BIAS} = 0V		0.6	1	mA	
ES5609 V_{IN} Quiescent when Active		$V_{EN/UV}$ = 2V, V_{FB} > 0.97V, $V_{SYNC/MODE}$ = 2V, V_{BIAS} = 0V		0.75	1.2	mA	
ES5609 Error Amp Transconductance	gm	V_{COMP}= 1.25V		1.7		mmho	
ES5609 COMP Source Current		V_{FB} = 0.77V, V_{COMP} = 1.25V		280		μA	
ES5609 COMP Sink Current		V_{FB} = 1.17V, V_{COMP} = 1.25V		280		μA	
ES5609 COMP Pin to Switch Current Gain				8		A/V	
ES5609 COMP Clamp Voltage				2.2		V	
BIAS Pin Current Consumption		V_{BIAS} = 3.5V, F_S = 2MHz, V_{IN} = 24V		29		mA	
EN/UV Rising Threshold	V_{ENR}		0.98	1.03	1.08	V	Y
EN/UV Pin Hysteresis	$V_{HYS(EN)}$			60		mV	
EN/UV Leakage Current	$I_{LKG(EN)}$	V_{EN} = 2V			±20	nA	
SOFT-START							
TK/SS Pin Source Current	$I_{TK/SS}$		1	2	3	μA	Y
TK/SS Pin Pull-Down Resistance		Fault Condition, TK/SS = 0.1V		300		Ω	
Internal Soft-Start Time	$t_{TK/SS}$	Float the TK/SS Pin		1		ms	
OUTPUT							
Regulated Feedback Voltage	V_{FB}	V_{IN} = 6V	966	970	974	mV	
		V_{IN} = 6V	960	970	980	mV	Y
Feedback Leakage Current	$I_{LKG(FB)}$	V_{FB}=0.97V			±20	nA	Y
FB Load Regulation		I_{OUT} = 0.5A to 8A, V_{IN}=24V, V_{OUT} = 5V		0.1		%A	
FB Line Regulation		V_{IN} = 4.0V to 65V, COMP = 1.25V		0.004	0.025	%V	Y

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	FTR
SWITCHING FREQUENCY							
Programmable Switching Frequency	F_S	R_{RT} =232kΩ	160	200	240	kHz	Y
		R_{RT} =60.4kΩ	600	700	800	kHz	Y
		R_{RT} =16.9kΩ	1.6	2.0	2.4	MHz	Y
SYNC/MODE DC and Clock Low Level Voltage			0.7			V	Y
SYNC/MODE Clock High Level Voltage					1.5	V	Y
SYNC/MODE DC High Level Voltage			2.2		2.9	V	Y
Synchronizable Frequency Range		SYNC/MODE Pin = External Clock	200		2200	kHz	
Spread Spectrum Modulation Frequency Range		R_{RT} = 60.4kΩ		20		%	
Spread Spectrum Modulation Frequency				3		kHz	
POWER GOOD							
Power Good Upper Threshold Offset from V_{FB}	V_{PGU}	V_{FB} Rising	6.5	8	10.5	%	Y
Power Good Lower Threshold Offset from V_{FB}	V_{PGL}	V_{FB} Falling	-10.5	-8	-6.5	%	Y
PG Hysteresis				0.4		%	
PG Pin Leakage Current	I_{PG}	V_{PG} = 3.3V			±80	nA	Y
Power Bad Pull-Down Resistance	R_{PBAD}	V_{PG} = 0.1V		200	500	Ω	Y
POWER SWITCH							
High-side NMOS On-Resistance	R_{HON}	I_{SW} = 1A		50		mΩ	
Low-side NMOS On-Resistance	R_{LON}	I_{SW} = 1A		30		mΩ	
High-side NMOS Current Limit	I_{LIMH}		10.5	14	17.5	A	
Low-side NMOS Current Limit	I_{LIML}			8		A	
SW Leakage Current	I_{SWL}	V_{IN} = 24V, V_{SW} = 0V, 24V			±1.5	μA	
Minimum On-Time	$I_{ON(MIN)}$	I_{OUT} = 3A, V_{SYNC} = 2V		25	50	ns	Y
Minimum Off-Time	$I_{OFF(MIN)}$			75	100	ns	

Note 1: The ES5608/ES5609 is tested under pulsed load conditions such that $T_J \approx T_A$. The ES5608I/ES5609I is guaranteed over the full −40°C to 125°C internal operating temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

Note 2: FTR means Full Temperature Range.

BLOCK DIAGRAM

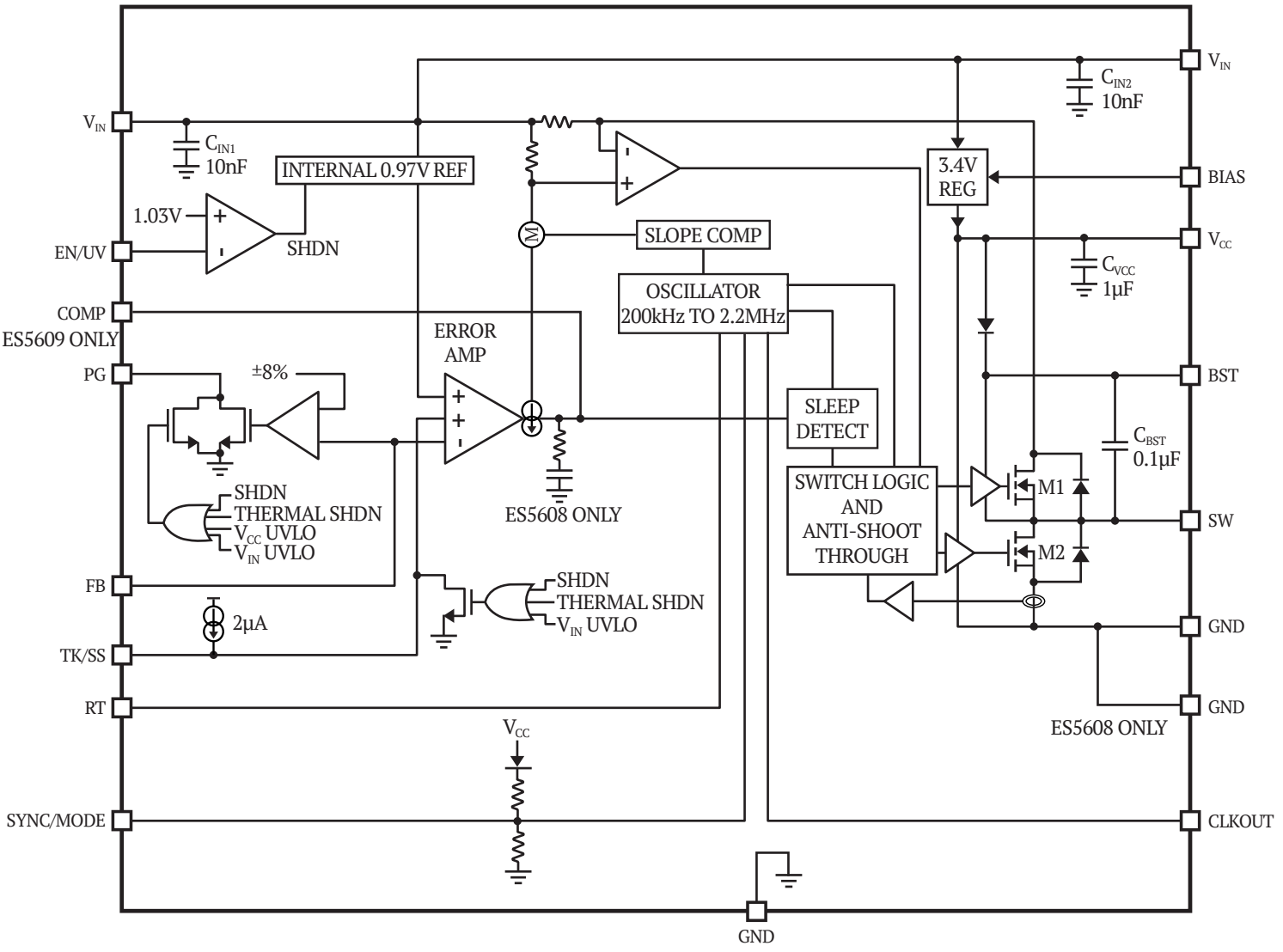
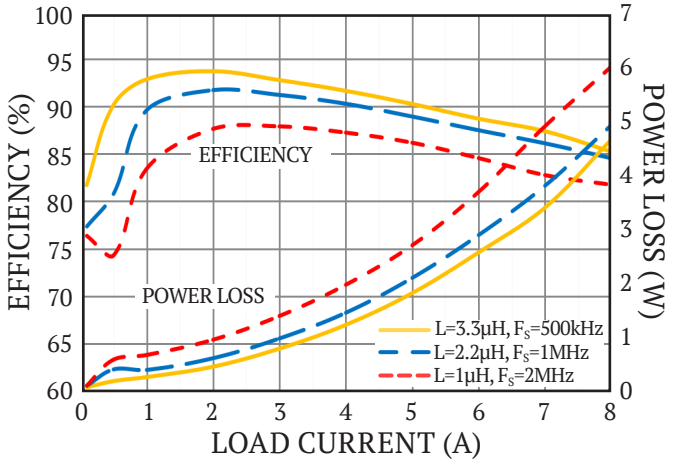


Figure 1 Simplified ES5608/ES5609 Internal Function Block Diagram

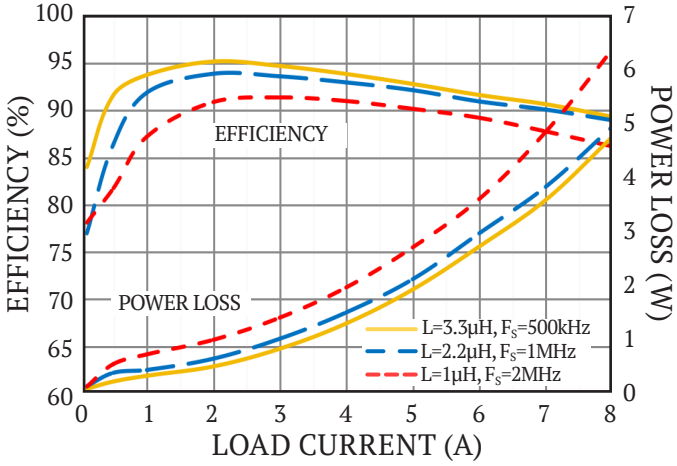
TYPICAL PERFORMANCE CHARACTERISTICS

12V_{IN} to 3.3V_{OUT} Efficiency Frequency



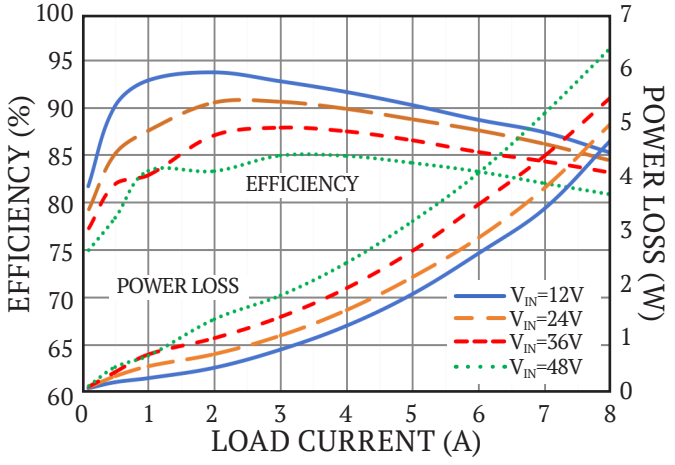
L: 74437358033, 3.3μH
74439344022, 2.2μH
74439344010, 1μH

12V_{IN} to 5V_{OUT} Efficiency Frequency



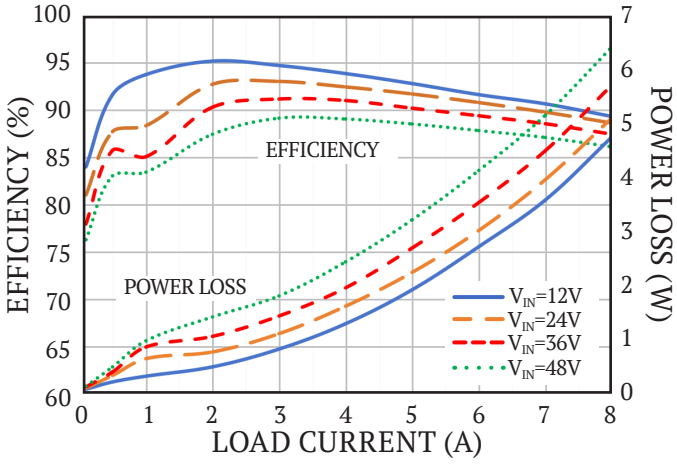
L: 74437358033, 3.3μH
74439344022, 2.2μH
74439344010, 1μH

Efficiency at 3.3V_{OUT}



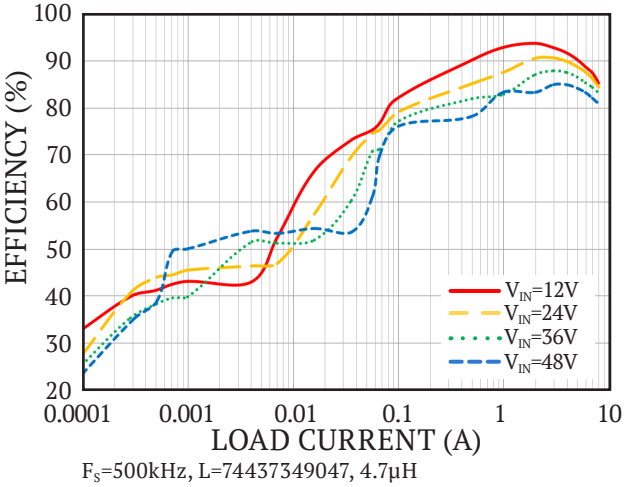
FS=500kHz, L=74437358033, 3.3μH

Efficiency at 5V_{OUT}



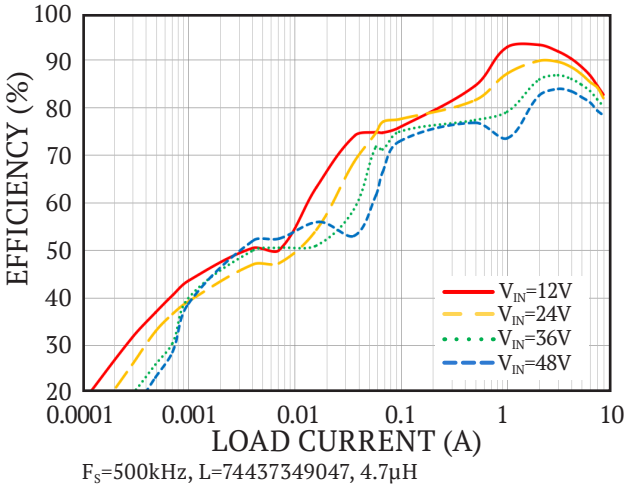
FS=500kHz, L=74437358033, 3.3μH

ES5608 Low Load Efficiency at 3.3V_{OUT}



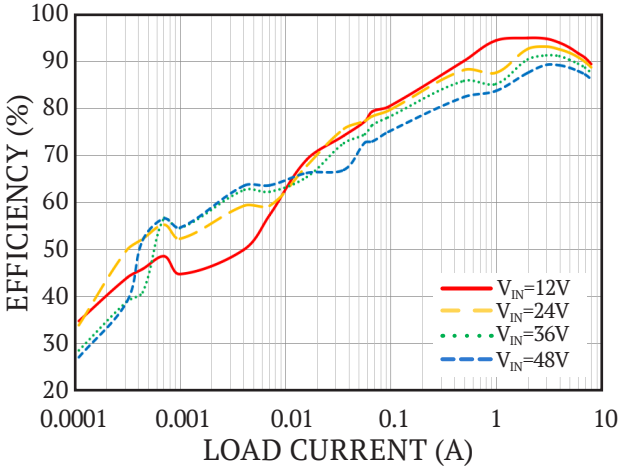
FS=500kHz, L=74437349047, 4.7μH

ES5609 Low Load Efficiency at 3.3V_{OUT}



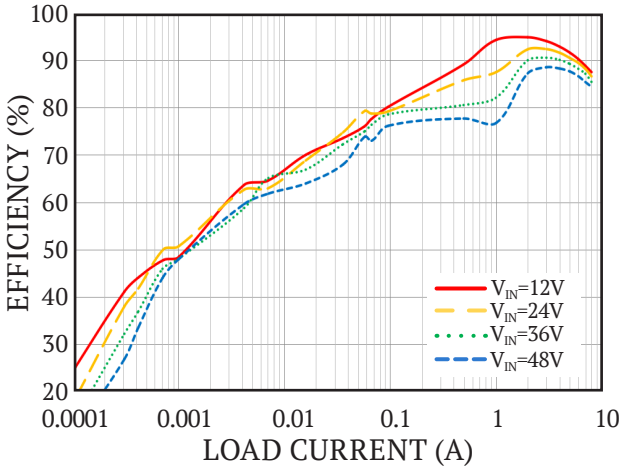
FS=500kHz, L=74437349047, 4.7μH

ES5608 Low Load Efficiency at $5V_{OUT}$



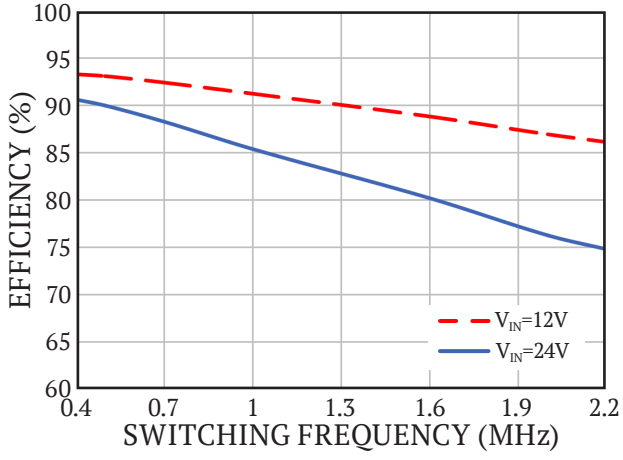
F_S=500kHz, L=74437349047, 4.7μH

ES5609 Low Load Efficiency at $5V_{OUT}$



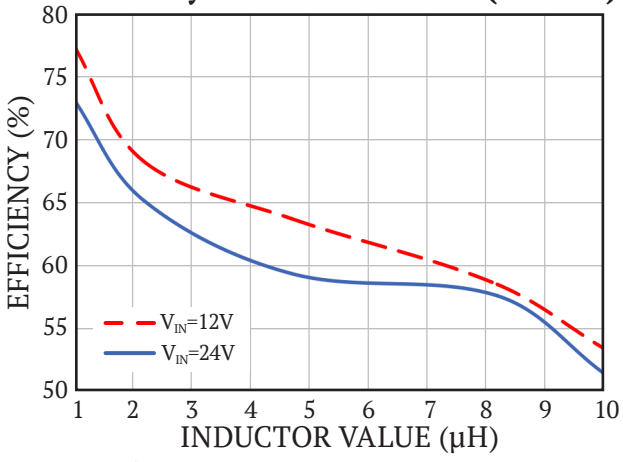
F_S=500kHz, L=74437349047, 4.7μH

Efficiency vs Frequency



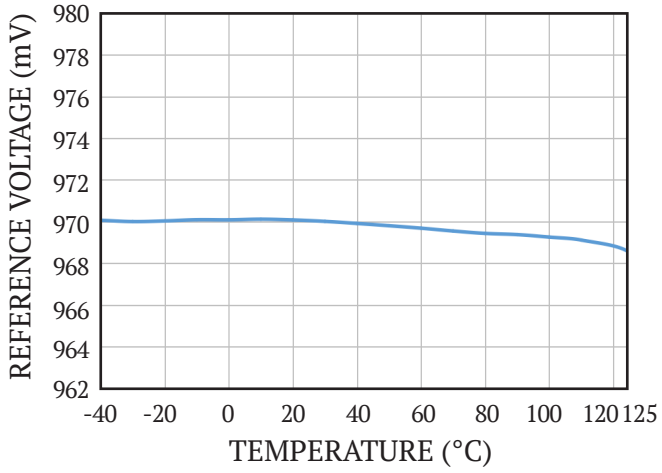
V_{OUT}=3.3V, I_{LOAD}=2A
L=74437349047, 4.7μH

Auto-sleep Mode Operation Efficiency vs Inductor Value (ES5608)

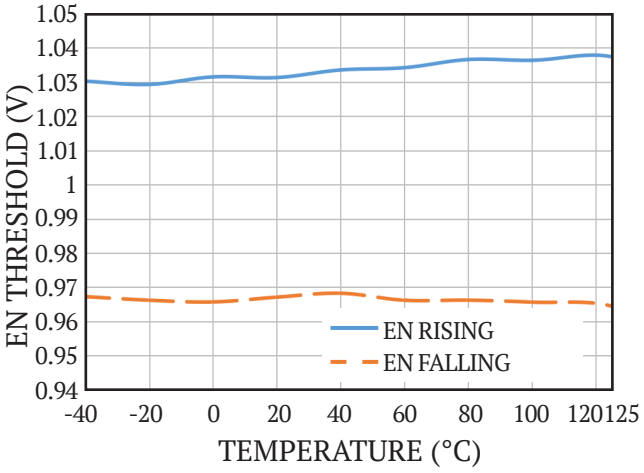


V_{OUT}=5V, I_{LOAD}=10mA
L=WE-LHMI7050

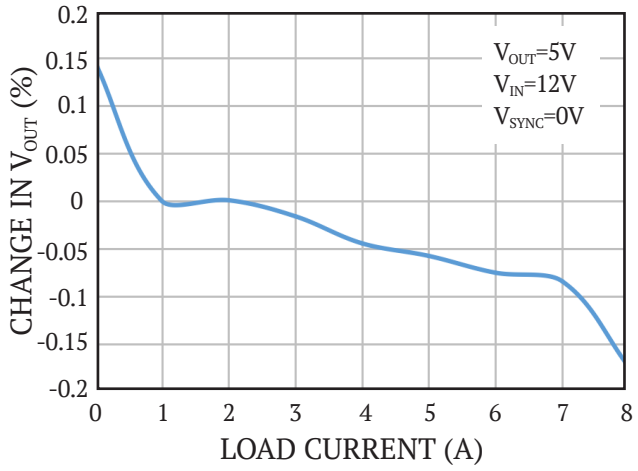
Regulated Feedback Voltage vs Temperature



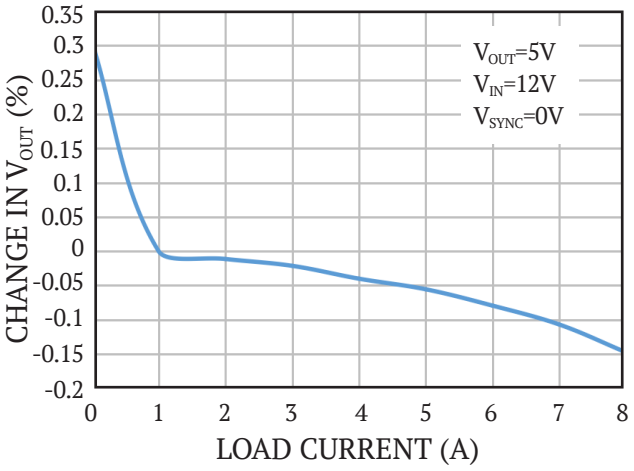
EN Pin Thresholds



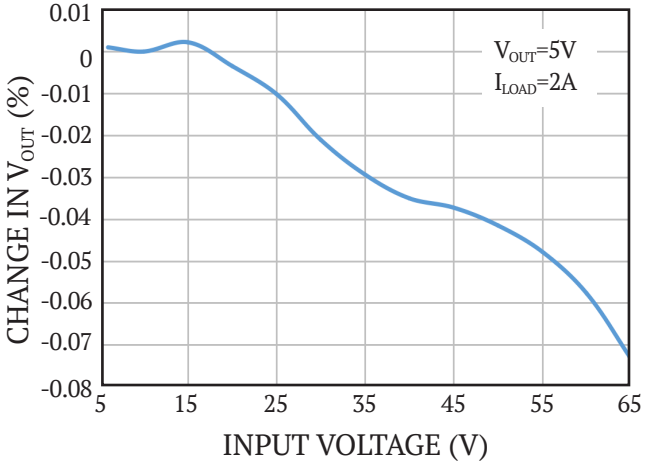
ES5608 Load Regulation



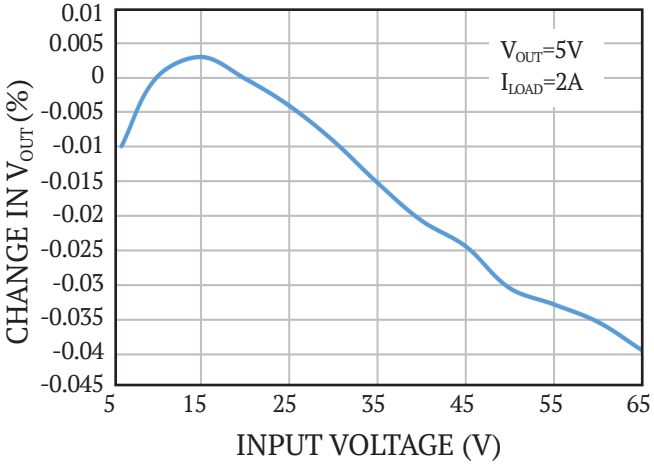
ES5609 Load Regulation



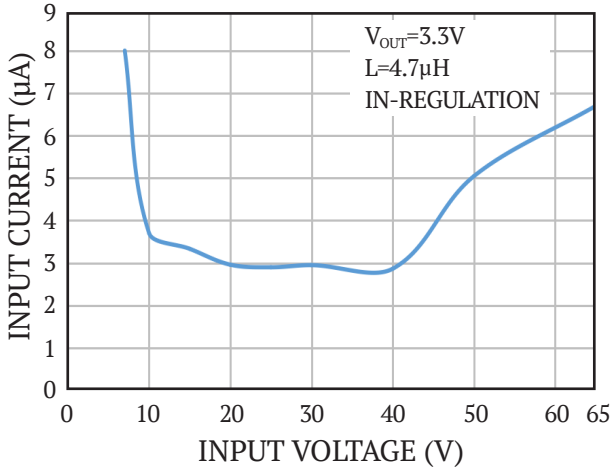
ES5608 Line Regulation



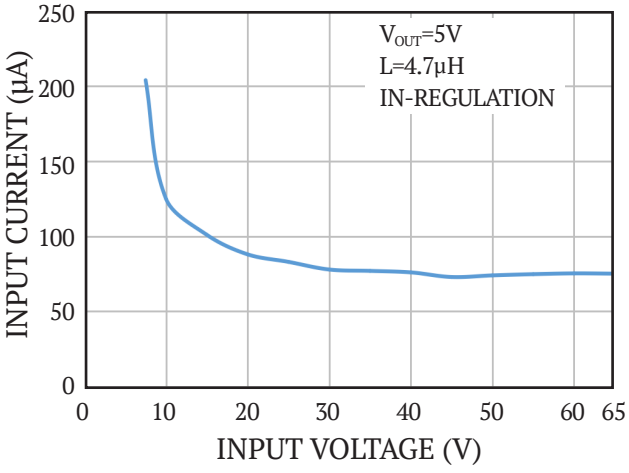
ES5609 Line Regulation



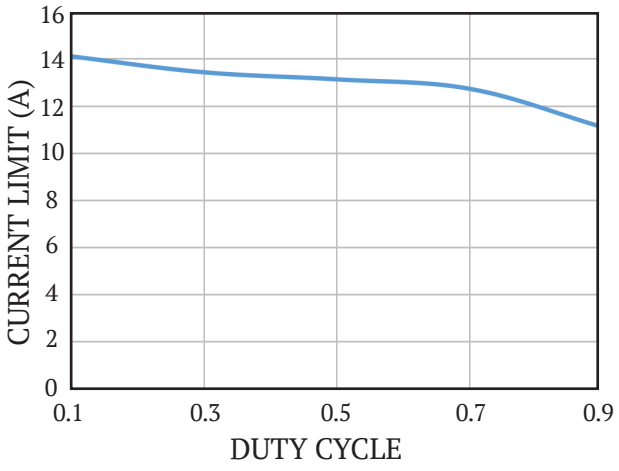
ES5608 No-Load Supply Current



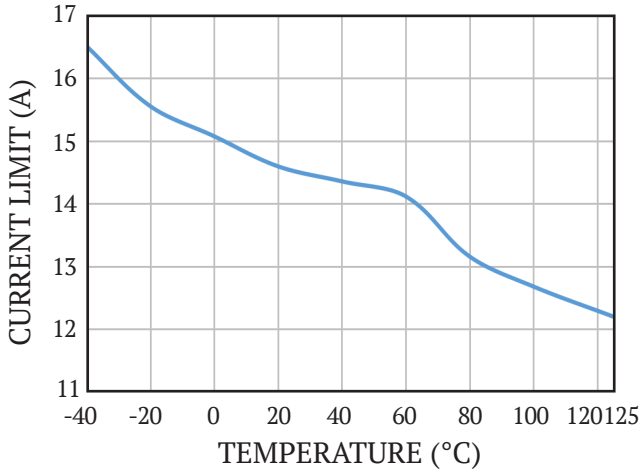
ES5609 No-Load Supply Current



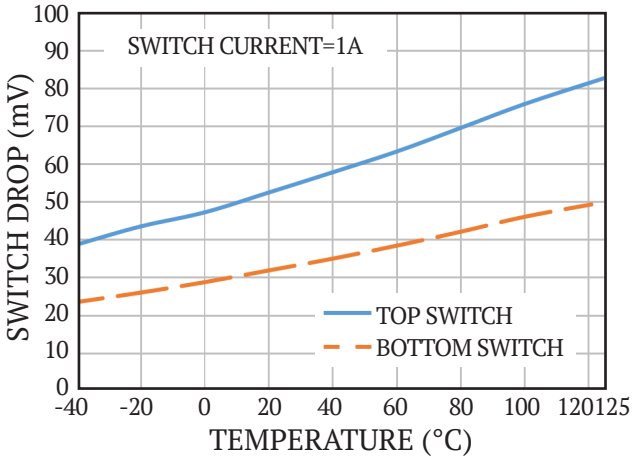
Top FET Current Limit vs Duty Cycle



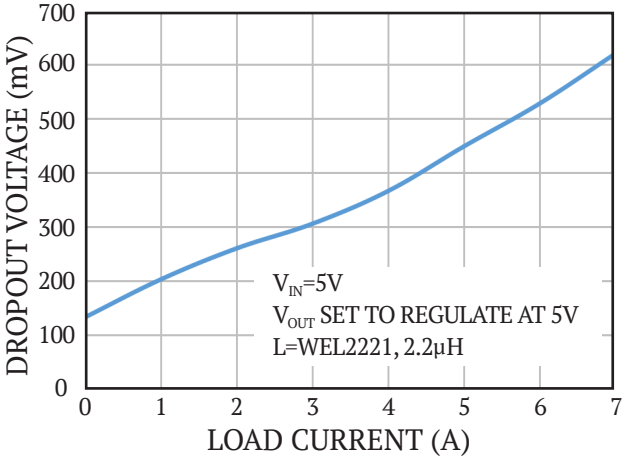
Top FET Current Limit vs Temperature



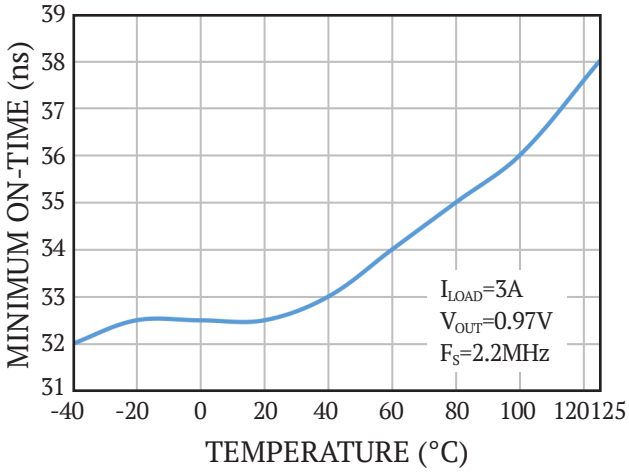
Switch Drop vs Temperature



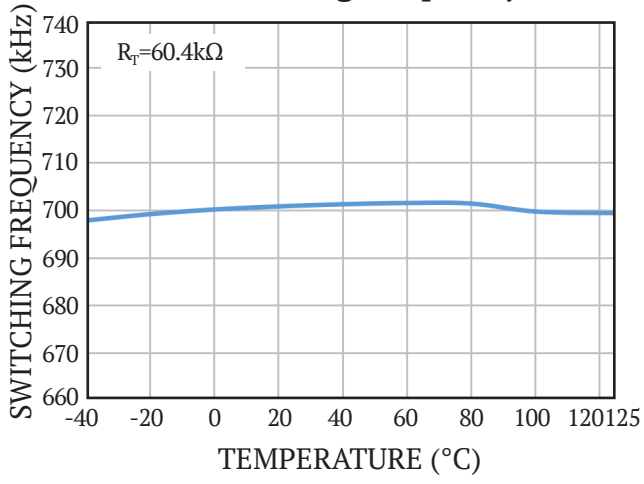
Dropout Voltage



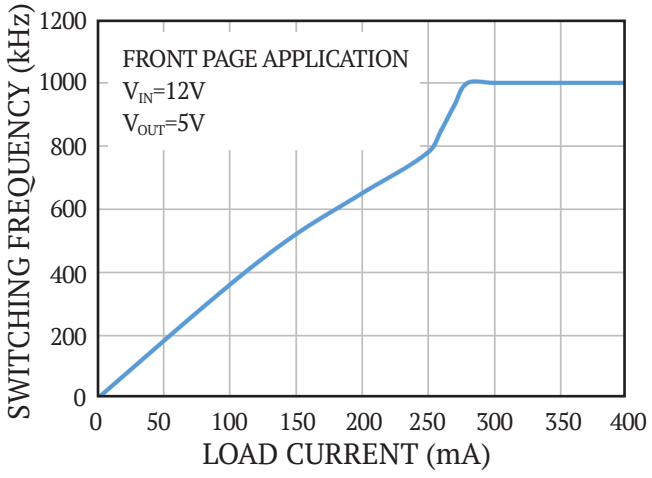
Minimum On-Time



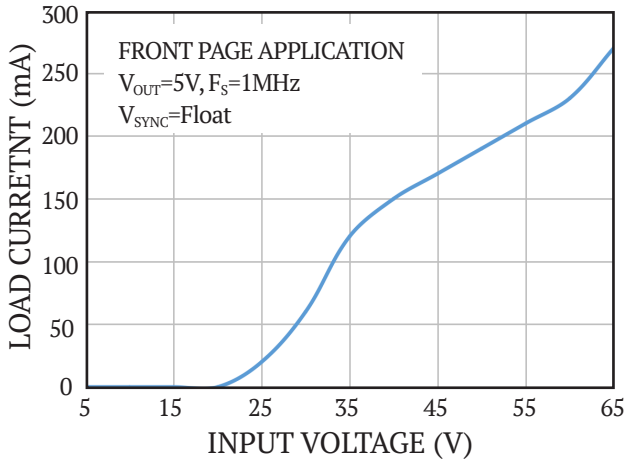
Switching Frequency



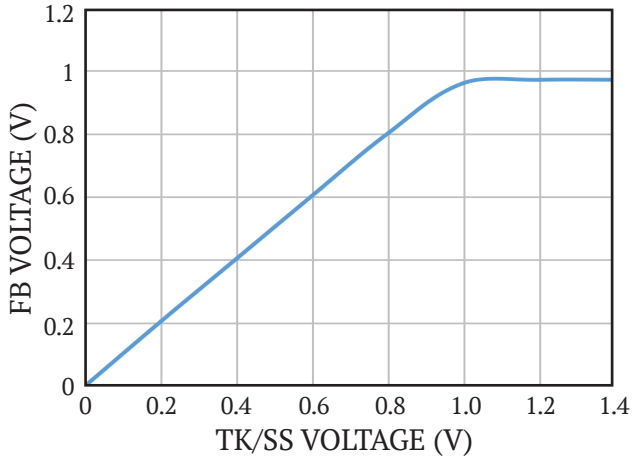
Auto-Sleep Mode Frequency vs Load Current



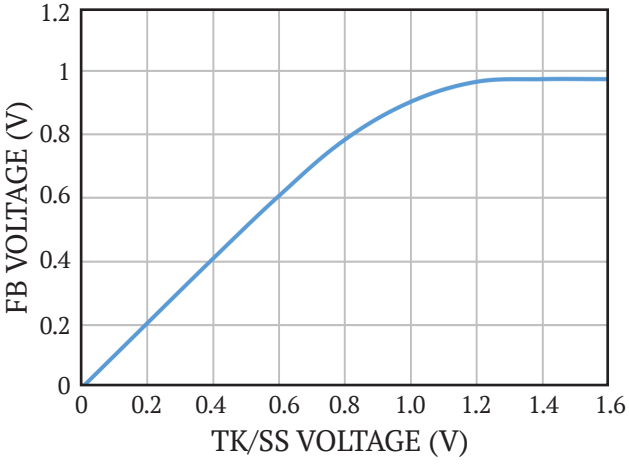
Auto-Sleep Mode Frequency vs Input Voltage



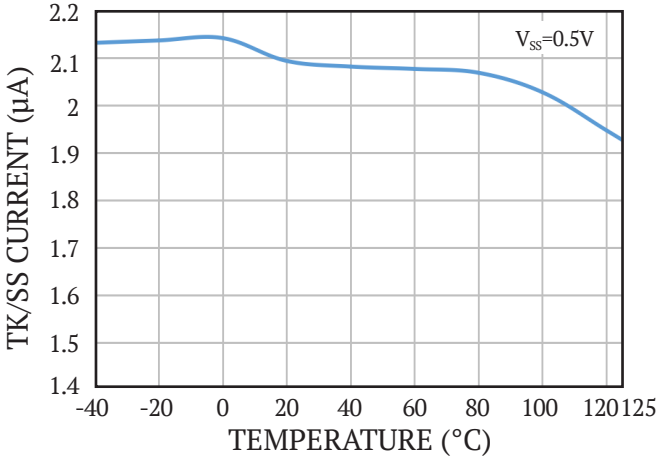
ES5608 Soft-Start Tracking



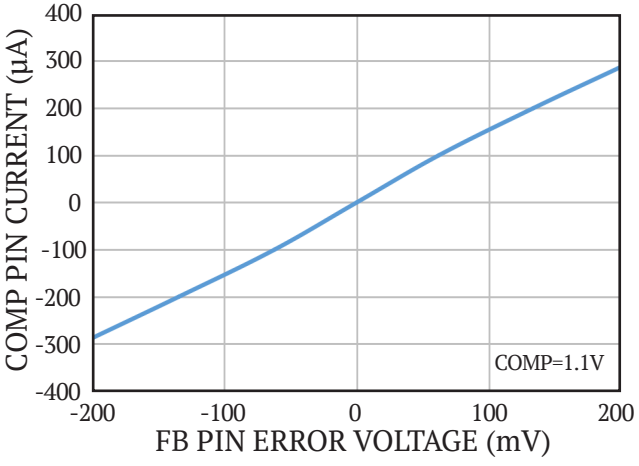
ES5609 Soft-Start Tracking



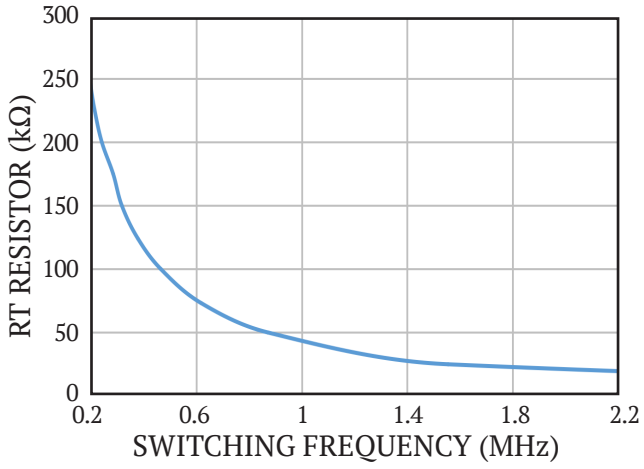
Soft-Start Current



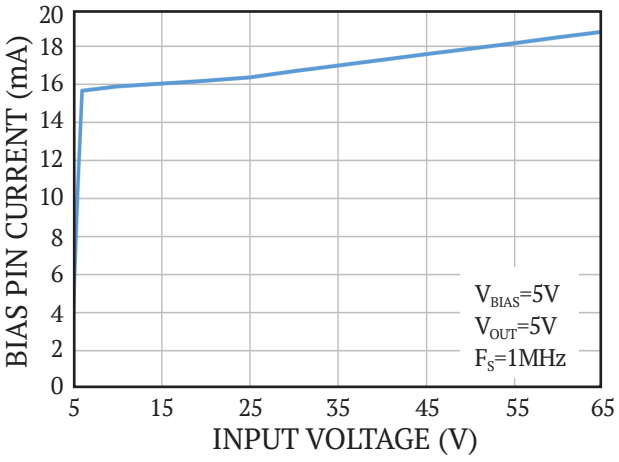
ES5609 Error Amp Output Current



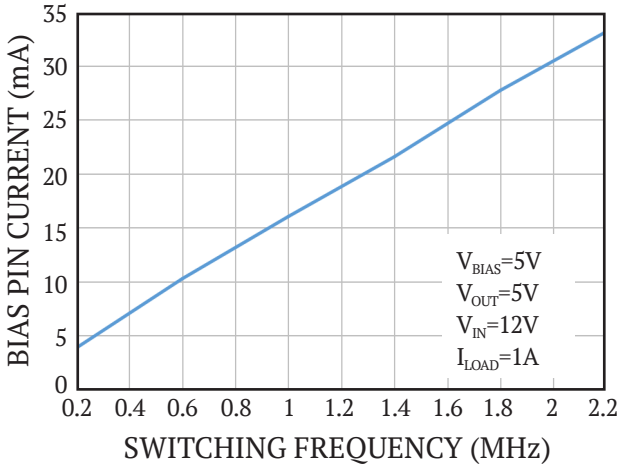
RT Programmed Switching Frequency



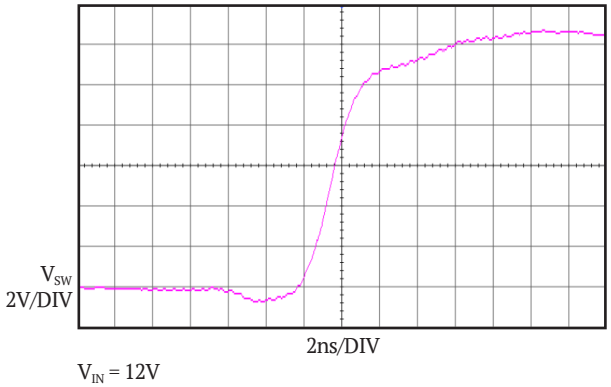
Bias Pin Current vs Input Voltage



Bias Pin Current vs Switching Frequency

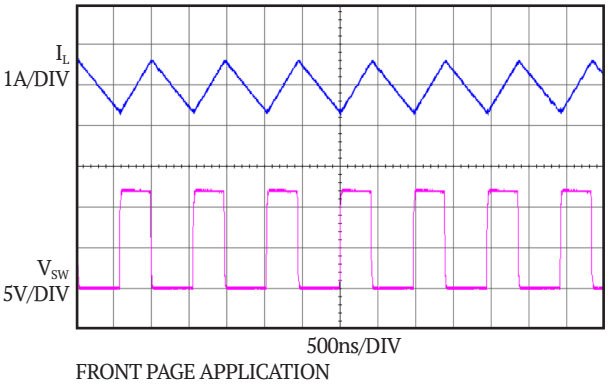


Switch Rising Edge



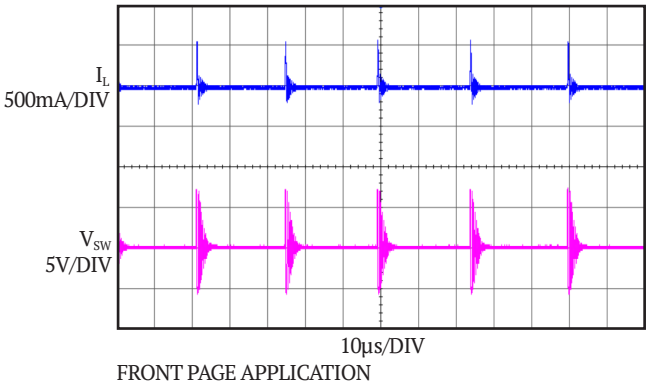
V_{IN} = 12V
I_{LOAD}=3A

Switching Waveforms, FCM Operation



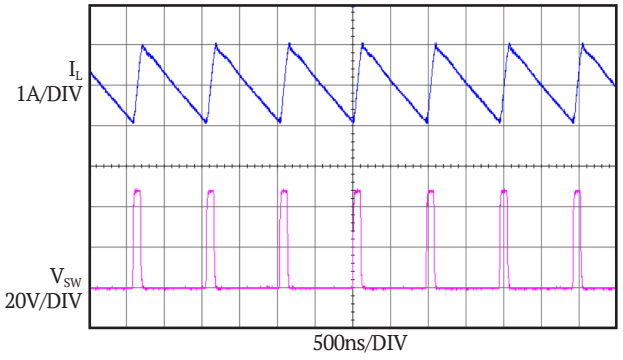
FRONT PAGE APPLICATION
$12V_{IN}$ TO $5V_{OUT}$ AT 2A

Switching Waveforms, Auto-sleep Mode Operation



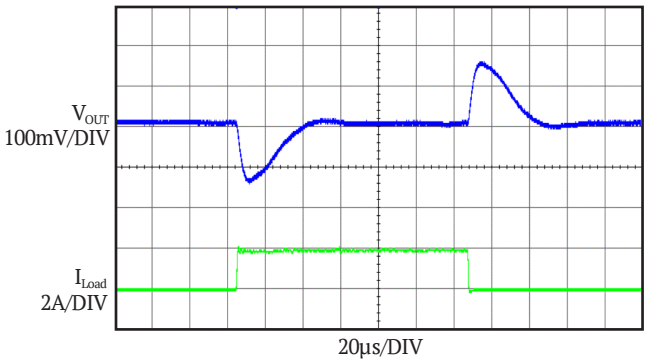
FRONT PAGE APPLICATION
$12V_{IN}$ TO $5V_{OUT}$ AT 10mA
V_{SYNC}=0V

Switching Waveforms



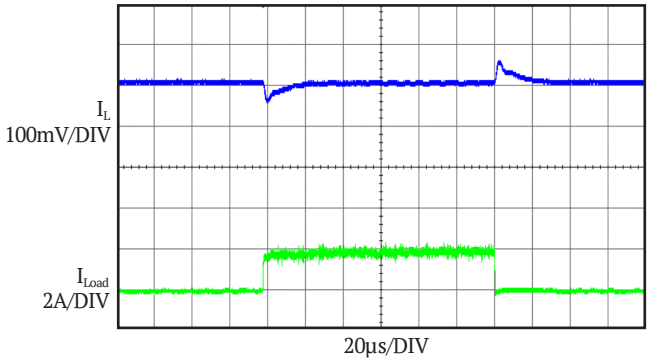
FRONT PAGE APPLICATION
$48V_{IN}$ TO $5V_{OUT}$ AT 2A

ES5608 Transient Response, FCCM



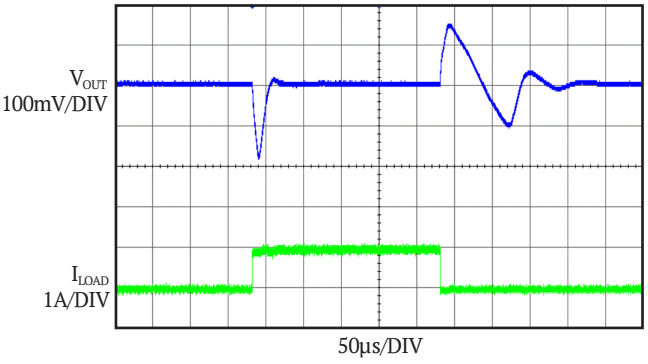
2A TO 4A TRANSIENT
$12V_{IN}$, $5V_{OUT}$, F_S=2MHz
C_{OUT}=2×47µF, C_{FF}=10pF

ES5609 Transient Response, FCCM



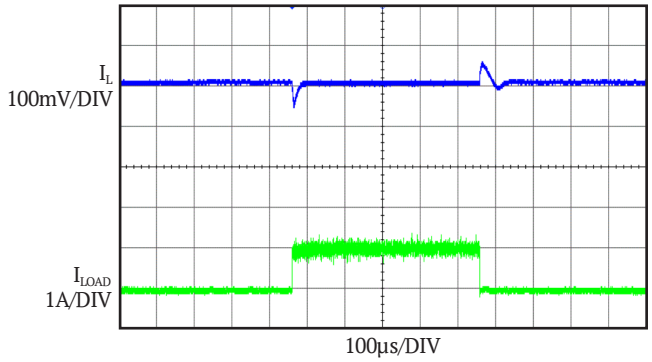
2A TO 4A TRANSIENT
C_{OUT}=2×47µF, C_{FF}=10pF
$12V_{IN}$, $5V_{OUT}$, F_S=2MHz, C_C=560pF, R_C=7.5kΩ

ES5608 Transient Response Auto Sleep Mode



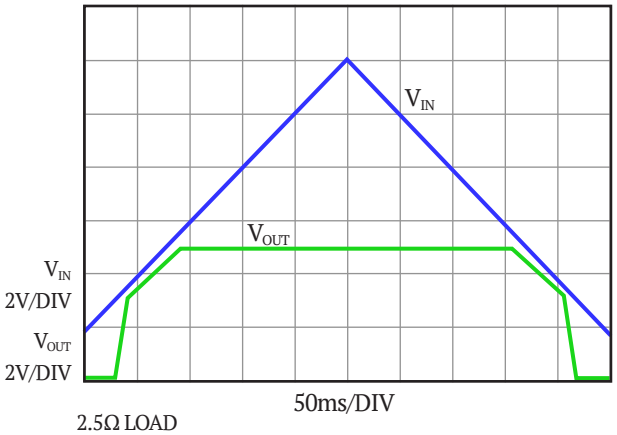
0.1A TO 1.1A TRANSIENT
$12V_{IN}$, $5V_{OUT}$, F_S=2MHz
C_{OUT}=2×47µF, C_{FF}=10pF

ES5609 Transient Response Auto Sleep Mode



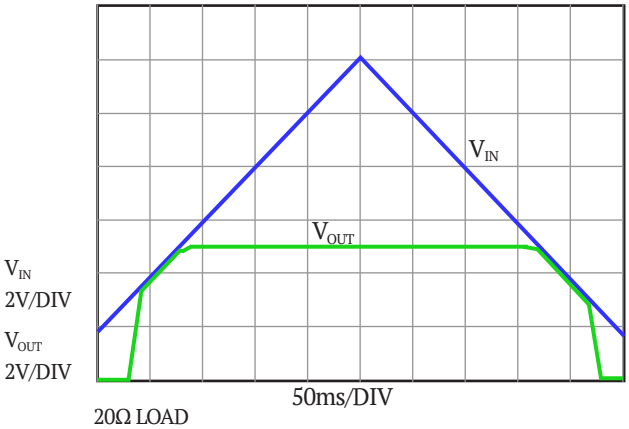
0.1A TO 1.1A TRANSIENT
C_{OUT}=2×47µF, C_{FF}=10pF
$12V_{IN}$, $5V_{OUT}$, F_S=2MHz, C_C=560pF, R_C=7.5kΩ

Start-Up Dropout Performance



2.5Ω LOAD
(2A IN REGULATION)

Start-Up Dropout Performance



20Ω LOAD
(250mA IN REGULATION)

DETAILED DESCRIPTION

GENERAL FEATURES

The ES5608/ES5609 is a monolithic, constant frequency high efficiency, synchronous buck converter operating over a wide input range from 3.2V to 65V. It uses peak current mode control architecture for easy loop compensation, excellent line and load regulation.

The ES5608/ES5609 can operate over a wide switching frequency range, including sub-AM band at 200kHz and above AM band at 2.2MHz with the correct resistor selection from the RT pin to ground. To further reduce EMI/EMC emission, a triangle spread spectrum switching modulation can be enabled with the SYNC/MODE pin.

The fast, clean, low overshoot switching edges enable high efficiency operation even at high switching frequencies, leading to a small overall solution size. Peak current mode control with a 25ns minimum on-time allows high step-down ratios even at high switching frequencies.

The ES5608/ES5609 comes in a 4×6mm LQFN package with input and boost capacitors integrated to achieve excellent EMI performance by reducing layout sensitivity.

ENABLE CONTROL

The ES5608/ES5609 has a precision enable control input. When the EN pin voltage is greater than 1.03V, the ES5608/ES5609 is enabled. If the EN pin is pulled below 0.97V, the device is disabled. When the EN pin is pulled low, the ES5608/ES5609 enters shutdown mode with a typical 2.4μA quiescent current.

CONTROL LOOP

The ES5608/ES5609 uses the output voltage information and the inductor current information to regulate the output voltage. The output voltage is sensed through a resistor divider from the FB pin to ground. The sensed signal is compared with internal 0.97V reference and the voltage difference is amplified by a transconductance amplifier to the COMP pin for the ES5609 and to the COMP signal inside the ES5608. The COMP pin or COMP signal indicates the target peak inductor current. If the output voltage decreases, the ES5608/ES5609 increases the target inductor peak current to raise the output voltage; if the output rises, the ES5608/ES5609 decreases the target peak inductor current to reduce the output voltage.

At the beginning of each clock cycle, the high-side power MOSFET is turned on. When the inductor current reaches the peak current value set by the COMP pin or COMP signal, the high-side power MOSFET is turned off; the low-side power MOSFET is turned on until the next clock cycle begins or the inductor current falls to zero. The controller regulates the output voltage by repeating this operation.

V_{CC} LOW DROPOUT REGULATOR (LDO) AND BIAS

The ES5608/ES5609 integrates one high performance, low dropout linear 3.4V V_{CC} regulator, which powers most blocks. The input voltage V_{IN} can be high up to 65V. Connect a minimum 1μF low ESR ceramic capacitor from the output V_{CC} to ground. The V_{CC} can supply enough current for the ES5608/ES5609's circuitry. To improve efficiency, the internal LDO can also draw current from the BIAS pin when the BIAS pin is at 3.3V or higher. Typically the BIAS pin can be tied to the output of the ES5608/ES5609, or can be tied to an external supply of 3.3V or above. If BIAS is connected to a supply other than $V_{OUT,}$ be sure to bypass with a local ceramic capacitor. If the BIAS pin is below 3.1V, the internal LDO will consume current from V_{IN}. Applications with high input voltage and high switching frequency where the internal LDO pulls current from V_{IN} will increase die temperature because of the higher power dissipation across the LDO. Do not connect an external load to the V_{CC} pin.

START-UP

The ES5608/ES5609 incorporates an external TK/SS pin to smoothly ramp up the output to the desired voltage when the device is enabled. During start-up, an internal 2μA current source begins charging up the soft-start capacitor connected to the TK/SS pin. The voltage error amplifier reference voltage is clamped to the voltage on the TK/SS pin when the TK/SS pin voltage is less than 0.97V. Therefore, the output voltage rises from 0V to regulation. The TK/SS pin can also be used for tracking. The soft start time can be calculated based on the function below:

$$t_{SS} = \frac{0.97V \cdot C_{SS}(\mu F)}{2\mu A}$$

When the soft-start time set by the external capacitor is less than 1ms, an internal soft-soft circuit of 1ms takes over the soft-start.
If the output is pre-biased to a certain voltage before start-up, the ES5608/ES5609 disables the switching of both the high-side and low-side power MOSFETs until the voltage on the TK/SS pin exceeds the FB pin voltage.

OPERATION MODE

The SYNC/MODE pin sets the operation mode. When the SYNC/MODE pin is floated or a clock signal is applied to the SYNC/MODE pin, the DCM is selected. In DCM, both the clock and all other internal circuits stay awake all the time. The switching cycle is aligned to the clock. The DCM is designed for fast transient response and full frequency operation over a wide load range. Negative inductor current is not allowed in DCM.
If the SYNC/MODE is pulled low to ground, the low ripple Auto-sleep mode operation is selected. The low-side power MOSFET turns off when the load current ramps to near zero in the Auto-sleep mode. The Auto-sleep mode is designed to enhance the light load efficiency. The ES5608/ES5609 has a minimum peak current limit setting in the Auto-sleep mode.
Once the load current is reduced to a lower value, the regulation is achieved by adjusting the frequency. With the loading current further reduced, the main internal circuitry may enter sleep mode for a while to achieve ultralow quiescent current. While in sleep mode, the ES5608 consumes 3μA and ES5609 consumes 140μA.
As the output load decrease, the percentage of time the ES5608/ES5609 is in sleep mode increases, resulting much higher light load efficiency than typical buck converters.

SPREAD SPECTRUM MODULATION

Switching regulators may be particularly troublesome for application when electromagnetic interface (EMI) is a concern. To improve the EMI, the ES5608/ES5609 can operate in spread spectrum mode by typing the SYNC/MODE pin to V_{CC}. This feature varies the switching frequency programmed by the RT pin to approximately 20% higher at low frequency rate, typically 3kHz with a triangular frequency modulation.
For example, when the ES5608/ES5609 is programmed at 2MHz and the spread spectrum modulation is activated, the switching frequency will vary between 2MHz and 2.4MHz at 3kHz rate. When the spread spectrum operation is selected, Auto-sleep operation is disabled, and the part will run in DCM.

SWITCHING FREQUENCY SELECTION

The switching frequency of the ES5608/ES5609 can be programmed in two methods: programming the frequency using an external resistor, synchronizing to an external clock.
Put a resistor between the RT pin and GND to program the switching frequency as shown in Table 1. Don't float the RT pin.

Table 1 SW Frequency vs R_T Value

F_S(MHz)	R_{RT}(kΩ)
0.2	232
0.3	150
0.4	110
0.5	88.7
0.6	71.5
0.7	60.4
0.8	52.3
1.0	40.2
1.2	33.2
1.4	26.7
1.6	22.6
1.8	19.6
2.0	16.9
2.2	14.7

When an external clock is applied to the SYNC/MODE pin, the ES5608/ES5609 switching frequency will automatically synchronize to the external clock. The RT resistor should be selected to set the ES5608/ES5609 switching frequency equal to or below the lowest synchronization clock. For example, if the synchronization clock is 700kHz and higher, the RT should be selected to be 60.4kΩ for 700kHz.

FB RESISTOR NETWORK OUTPUT VOLTAGE SETTING

The ES5608/ES5609 output voltage is set by the two resistors between the FB pin and V_{OUT}. The output voltage can be calculated by the function:

$$V_{OUT} = 0.97V \cdot \left(1 + \frac{R_1}{R_2}\right)$$

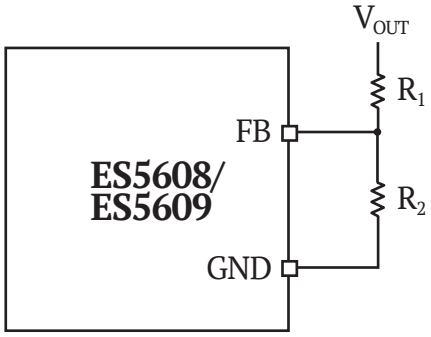


Figure 2 V_{OUT} Setting

When light load high efficiency is preferred, the total resistance of FB resistor divider should be chosen as large as possible because it is also a load on the output which consumes quiescent current. When using large FB resistors, a 1pF to 100pF phase-lead capacitor should be connected from V_{OUT} to FB.

POWER GOOD INDICATOR

The PG pin is an open drain power good indicator controlled by a windows comparator. If the regulated feedback voltage is within the ±8% window of the regulation point, the PG pin will be high impedance. The PG pin should be connected to V_{CC} or another voltage source through a typical 100kΩ resistor.

To prevent glitching both the upper and lower thresholds include 0.4% of hysteresis. PG is valid when V_{IN} is above 3V.

The PG pin is also actively pulled low during several conditions: EN/UV pin is below 0.97V, V_{CC} has fallen too low, V_{IN} is too low, or thermal shutdown.

OVERCURRENT PROTECTION

The ES5608/ES5609 features cycle-by-cycle high-side power MOSFET current limit. Whenever the high-side power MOSFET current limit is exceeded, the high-side power MOSFET is immediately turned off and low-side power MOSFET is turned on. The maximum high-side current limit is typically 14A at low duty cycles and decreases linearly to 12A at DC = 0.8. The inductor value must then be sufficient to supply the desired maximum output current.

The current through the low-side power MOSFET is also sensed while it is turned on. The maximum low-side overcurrent limit is typically 11A. If the low-side overcurrent limit is exceeded, the ES5608/ES5609 skips the next high-side turning on. The ES5608/ES5609 will not turn on the high-side power MOSFET until the low-side overcurrent threshold is no longer exceeded. If overload conditions result in more than 11A flowing through the bottom switch, the next clock cycle will be delayed until switch current returns to a safe level.

OVERTEMPERATURE PROTECTION

The internal overtemperature protection monitors the junction temperature of the ES5608/ES5609. If the junction temperature reaches approximately 160°C, the ES5608/ES5609 will stop switching and the TK/SS pin is pulled to ground. The ES5608/ES5609 goes back switching after the tie temperature reduces to be less than 140°C.

MINIMUM ON-TIME/OFF-TIME

The minimum on-time, $t_{ON(MIN)}$, is the smallest time that the ES5608/ES5609 is capable of turning of the high-side power MOSFET. It is determined by the gate charge and the internal timing delays. The minimum on-time design should meet the following equation:

$$t_{ON(MIN)} < \frac{V_{OUT}}{V_{IN} \cdot F_S}$$

The minimum on-time of the ES5608/ES5609 is 25ns. If the system design cannot meet the minimum on-time requirement, it will skip pulse.

Conversely, the minimum off-time is the smallest amount of time that ES5608/ES5609 can turn on the low-side power MOSFET. The ES5608/ES5609 is capable of maximum duty cycle approaching 99%, and the V_{IN} to V_{OUT} dropout is limited by the R_{DSON} of the high-side power MOSFET. In this mode, the ES5608/ES5609 skips switch cycles, resulting a lower switching frequency than the RT programmed frequency.

MULTI-IC PARALLELING

To increase the possible output current, two ES5609s can be connected in parallel to the same output. To do this, the COMP, TK/SS, and FB pins are connected together, and each ES5609's SW pin is connected to the common output through its own inductor. The CLKOUT pin of one ES5609 should be connected to the SYNC/

MODE pin of the second ES5609 to have both devices operate in the same mode.

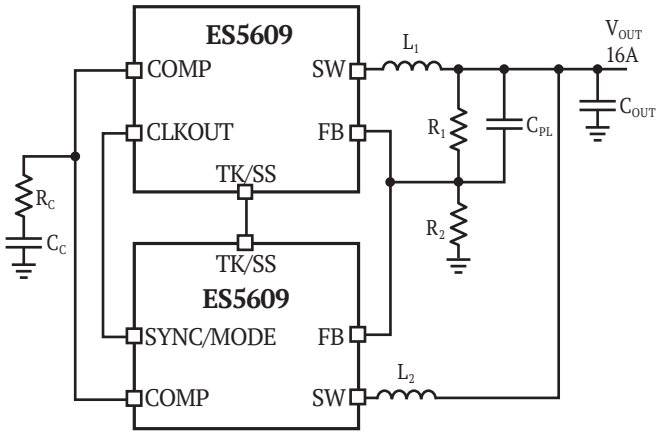


Figure 3 Paralleling Two ES5609s

During DCM, spread spectrum, and synchronization modes, both devices will operate at the same frequency. Figure 3 shows an application where two ES5609 are paralleled to obtain one output capable of up to 16A.

OUTPUT SHORT CIRCUIT PROTECTION

The ES5608/ES5609 will tolerate a shorted output. Several methods are used to protect the ES5608/ES5609 during output short-circuit conditions. The first method is the switching frequency will be folded back while the output is lower than the set point to maintain inductor current control. Second, the low-side power MOSFET's current is monitored such that if inductor current is beyond safe levels, the switching of the high-side power MOSFET will be delayed until such time as the inductor current falls to safe levels.

Frequency foldback behavior depends on the state of the SYNC/MODE pin: If the SYNC/MODE pin is low the switching frequency will slow when the output voltage is lower than the programmed level. If the SYNC/MODE pin is connected to a clock source, floated or tied high, the ES5608/ES5609 will stay at the programmed frequency without foldback and only slow switching if the inductor current exceeds safe levels.

DESIGN EXAMPLE

Figure 4 shows an ES5608/ES5609 in an application with the following specifications: $V_{IN(TYP)}$ = 24V, $V_{IN(MAX)}$ = 65V, V_{OUT} = 5V, $I_{OUT(MAX)}$ = 8A.

The output is set by:

$$V_{OUT} = 0.97V \cdot (1 + \frac{R_A}{R_B}) = 0.97V \cdot (1 + \frac{1M\Omega}{243k\Omega}) \approx 5V$$

Selecting the switching frequency is a tradeoff between solution size and efficiency. High switching frequency helps to reduce the solution size by using smaller output capacitors and inductors. However, it causes extra switching losses. For this application, 500kHz is selected by choosing 88.7kΩ resistor for the RT pin to ground.

For peak current mode control application, the typical inductor current ripple is between 20% and 40% of the maximum output current. The inductor value can be calculated if 30% is chosen as:

$$L = \frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{V_{IN} \cdot F_S \cdot 0.3 \cdot I_{OUT}}$$

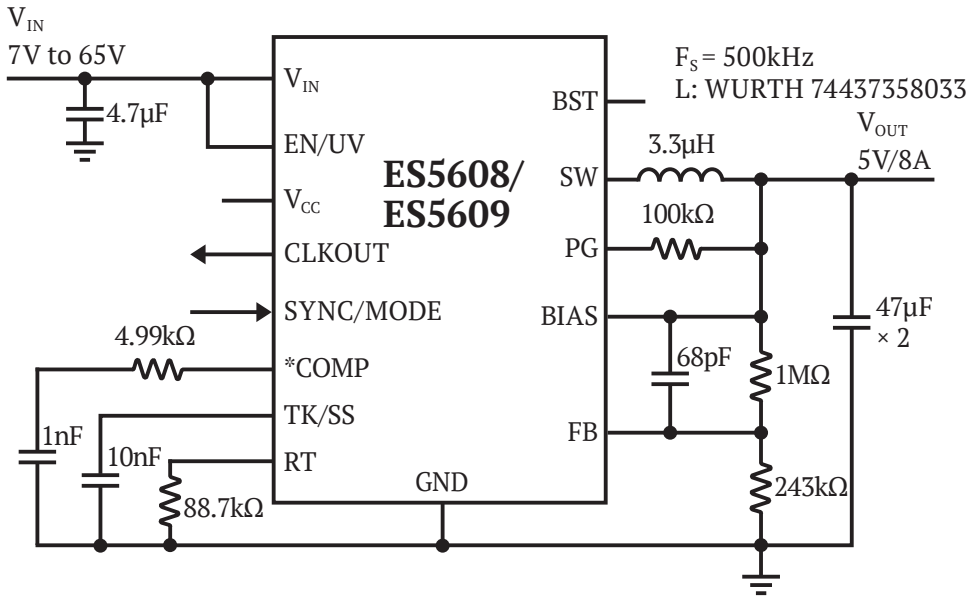
$$= \frac{5V \cdot (24V - 5V)}{24V \cdot 500kHz \cdot 0.3 \cdot 8A}$$

$$= 3.3\mu H$$

Choose 3.3µH WURTH 74437358033 inductor to ease the design.

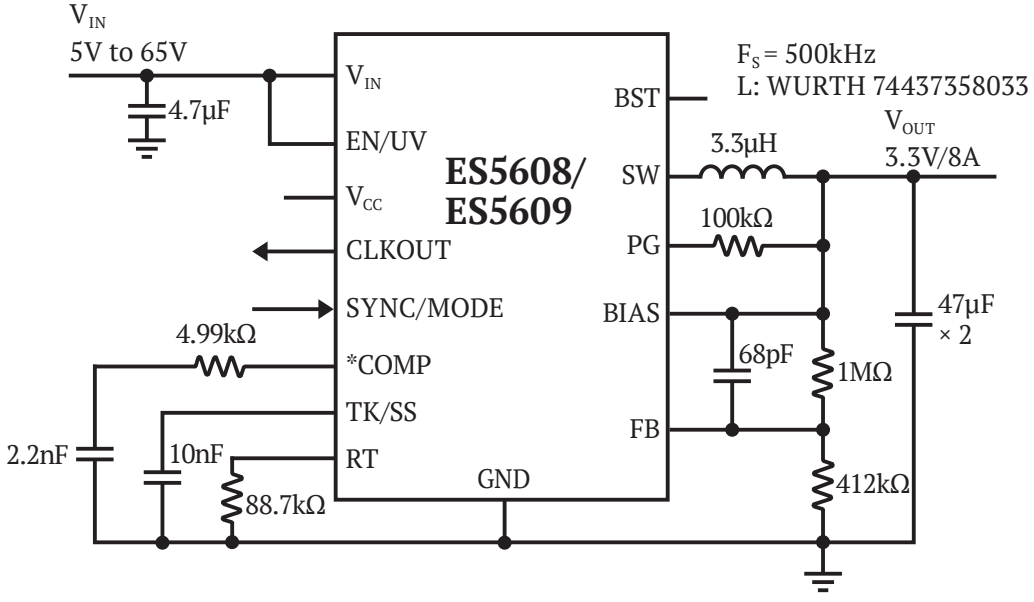
The TK/SS pin has 10nF capacitor for external soft-start purpose.

TYPICAL APPLICATION



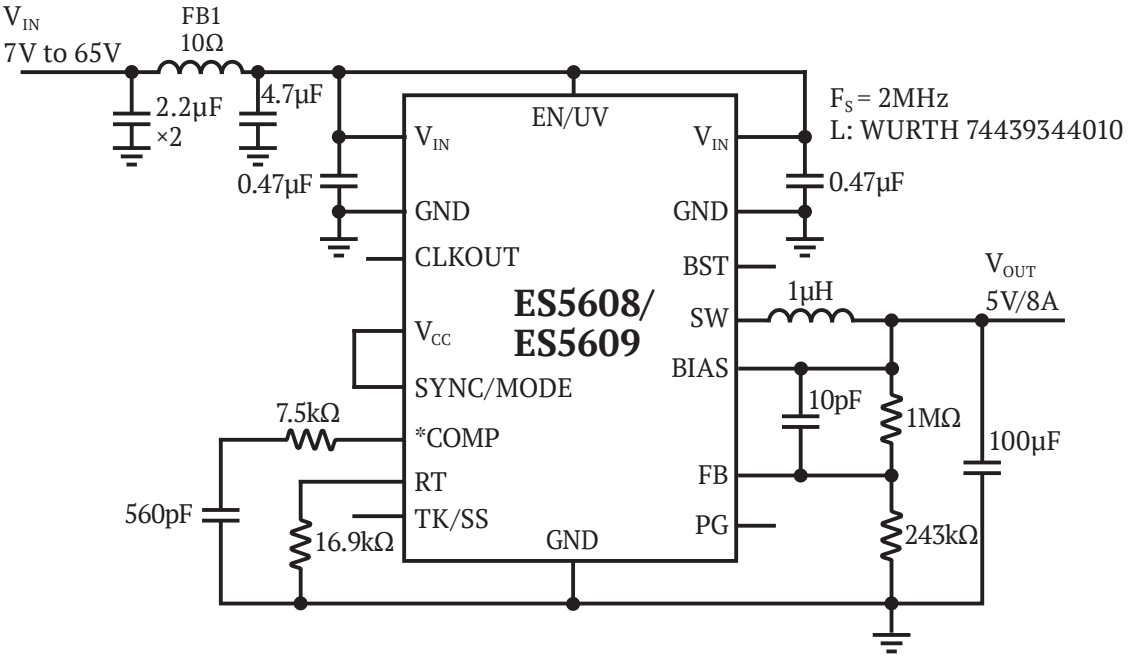
*COMP PIN AND COMPONENTS
ONLY APPLY TO ES5609

Figure 4 500kHz 5V, 8A Step-Down Converter with Soft-Start and Power Good



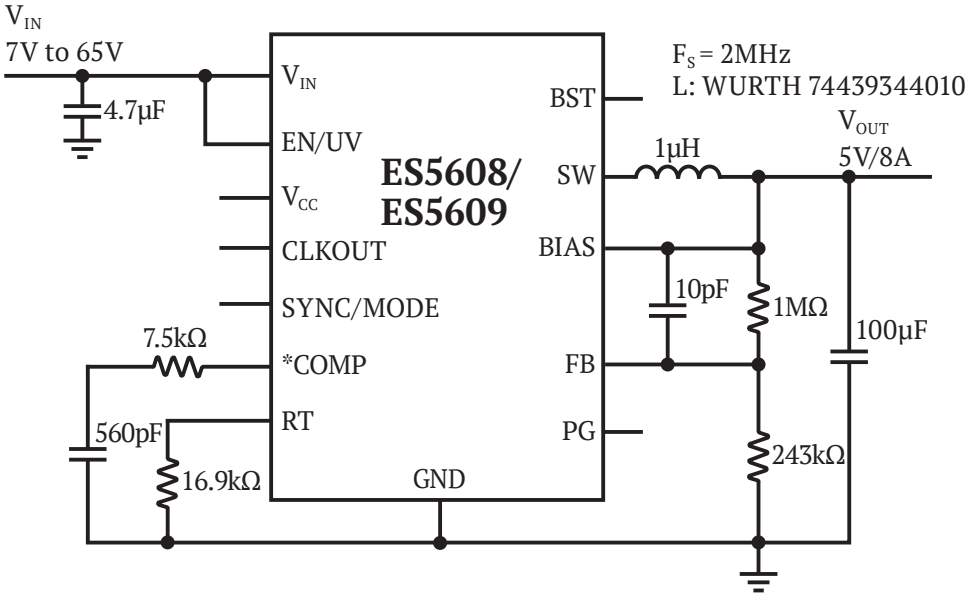
*COMP PIN AND COMPONENTS
ONLY APPLY TO ES5609

Figure 5 500kHz 3.3V, 8A Step-Down Converter with Soft-Start Power Good



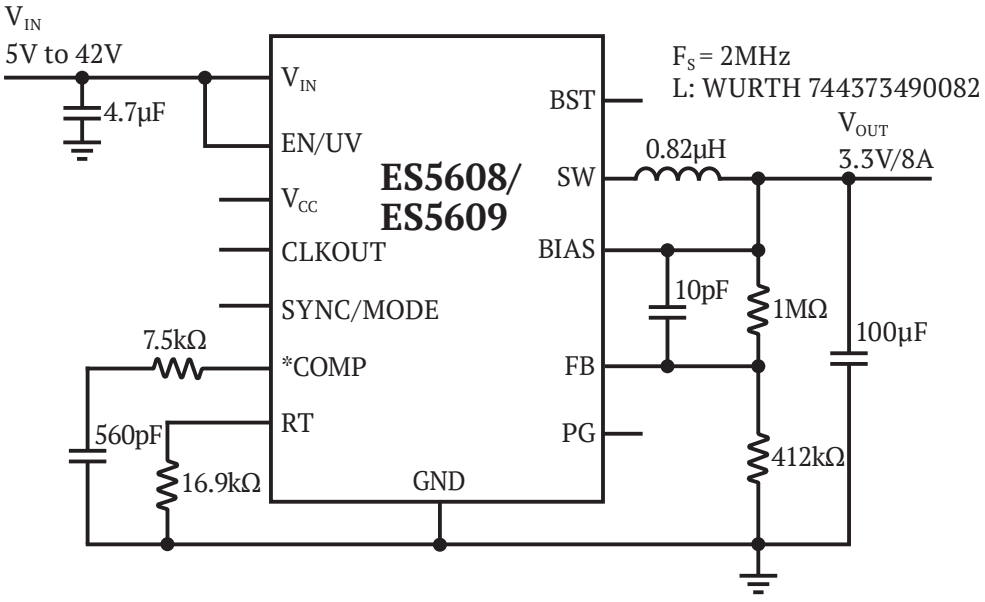
*COMP PIN AND COMPONENTS
ONLY APPLY TO ES5609

Figure 6 Ultralow EMI 5V, 8A Step-Down Converter with Spread Spectrum



*COMP PIN AND COMPONENTS
ONLY APPLY TO ES5609

Figure 7 2MHz 5V, 8A Step-Down Converter



*COMP PIN AND COMPONENTS
ONLY APPLY TO ES5609

Figure 8 2MHz 3.3V, 8A Step-Down Converter

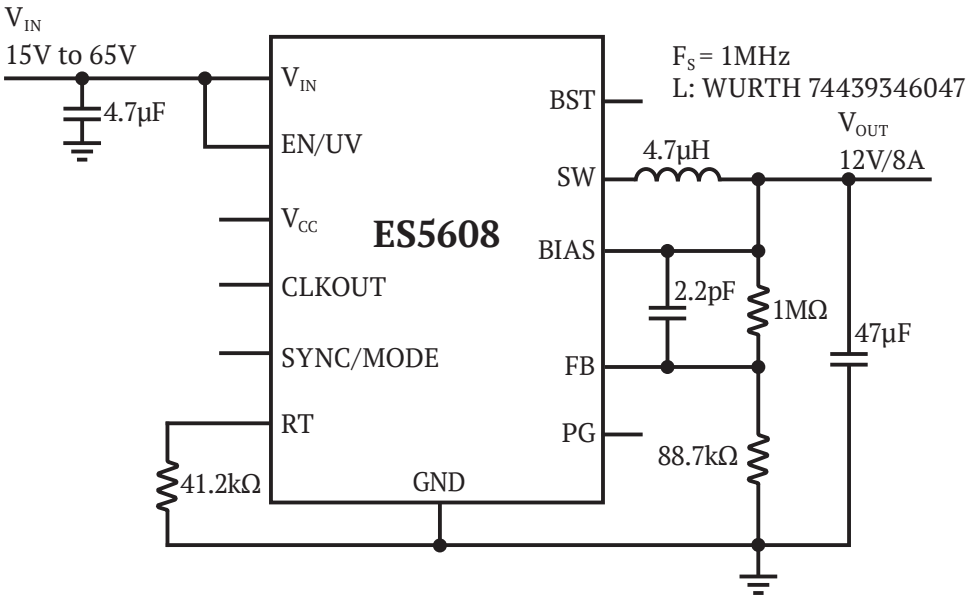
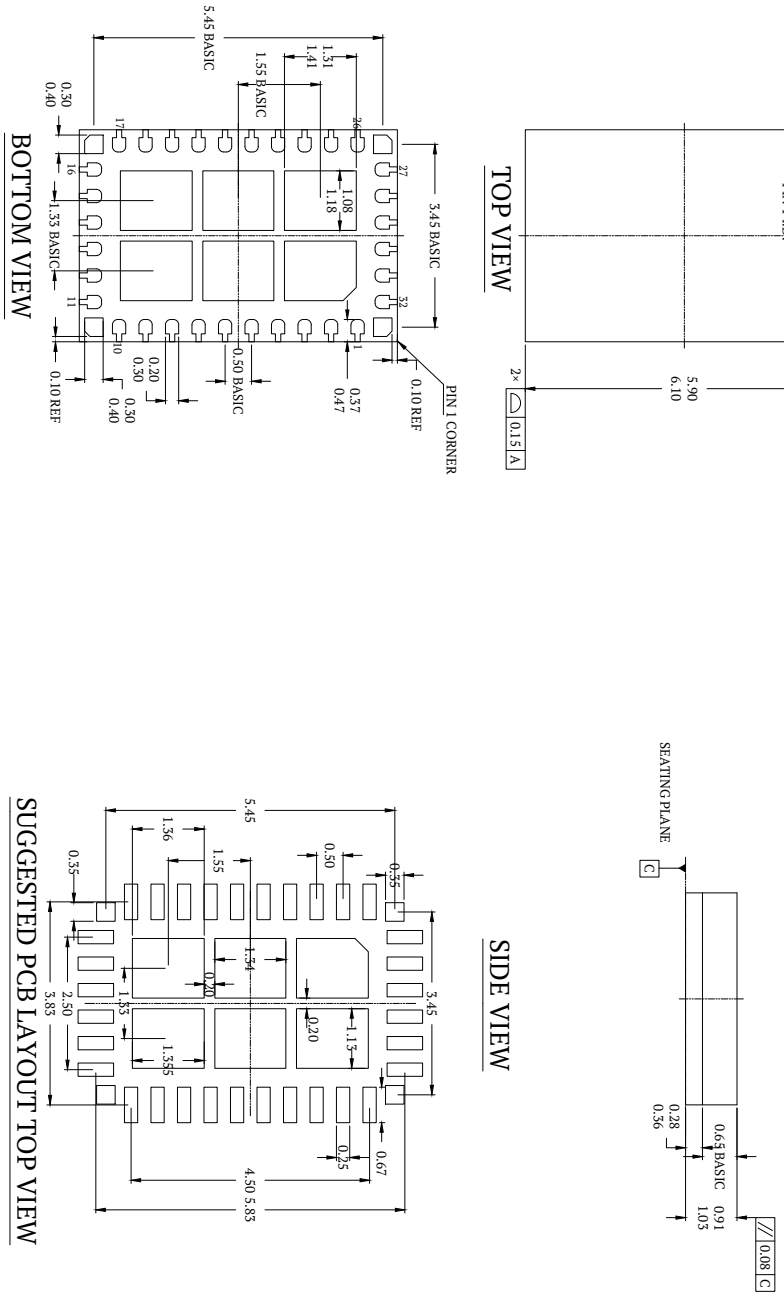
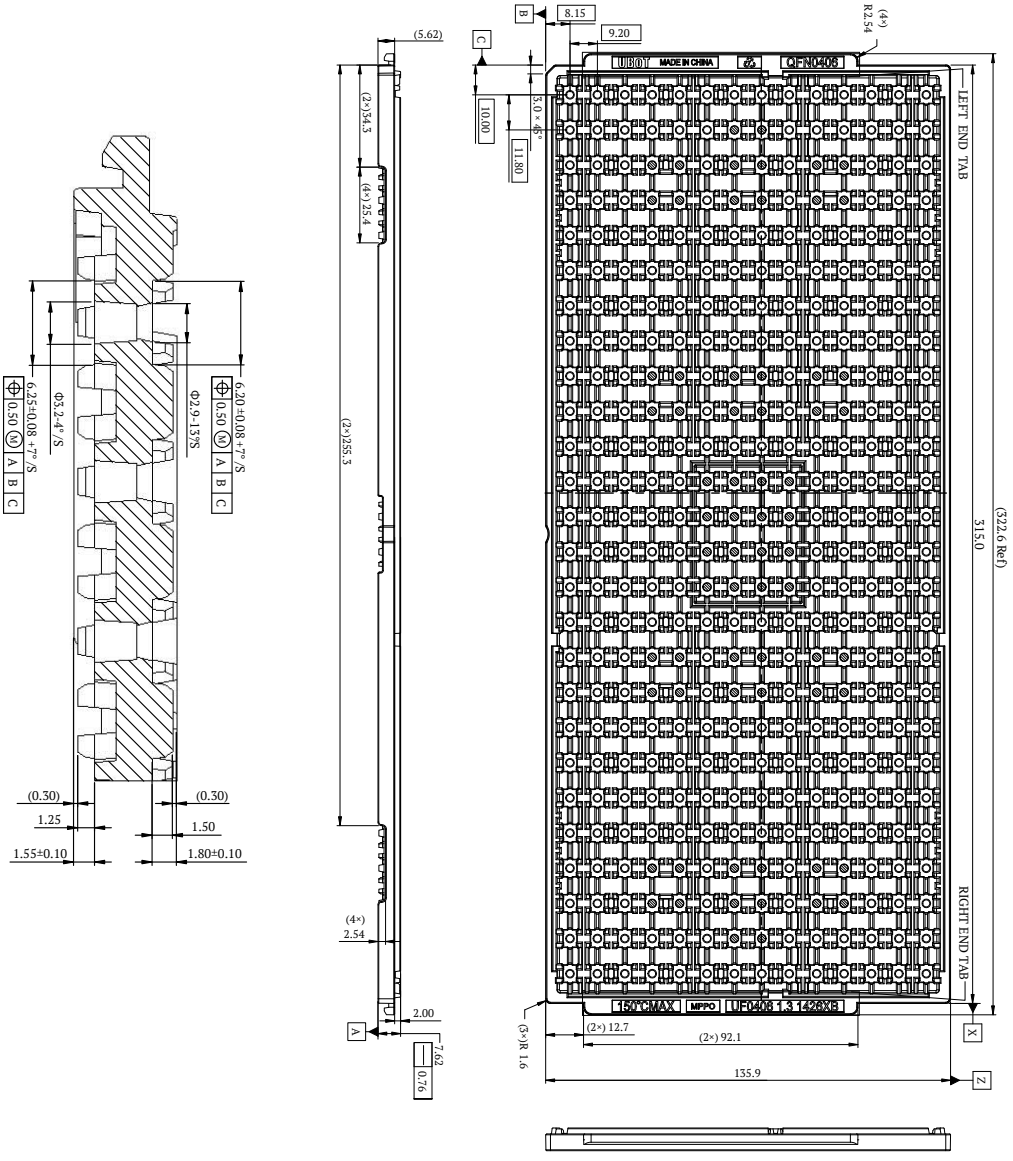


Figure 9 1MHz 12V, 8A Step-Down Converter

PACKAGE OUTLINE DRAWING

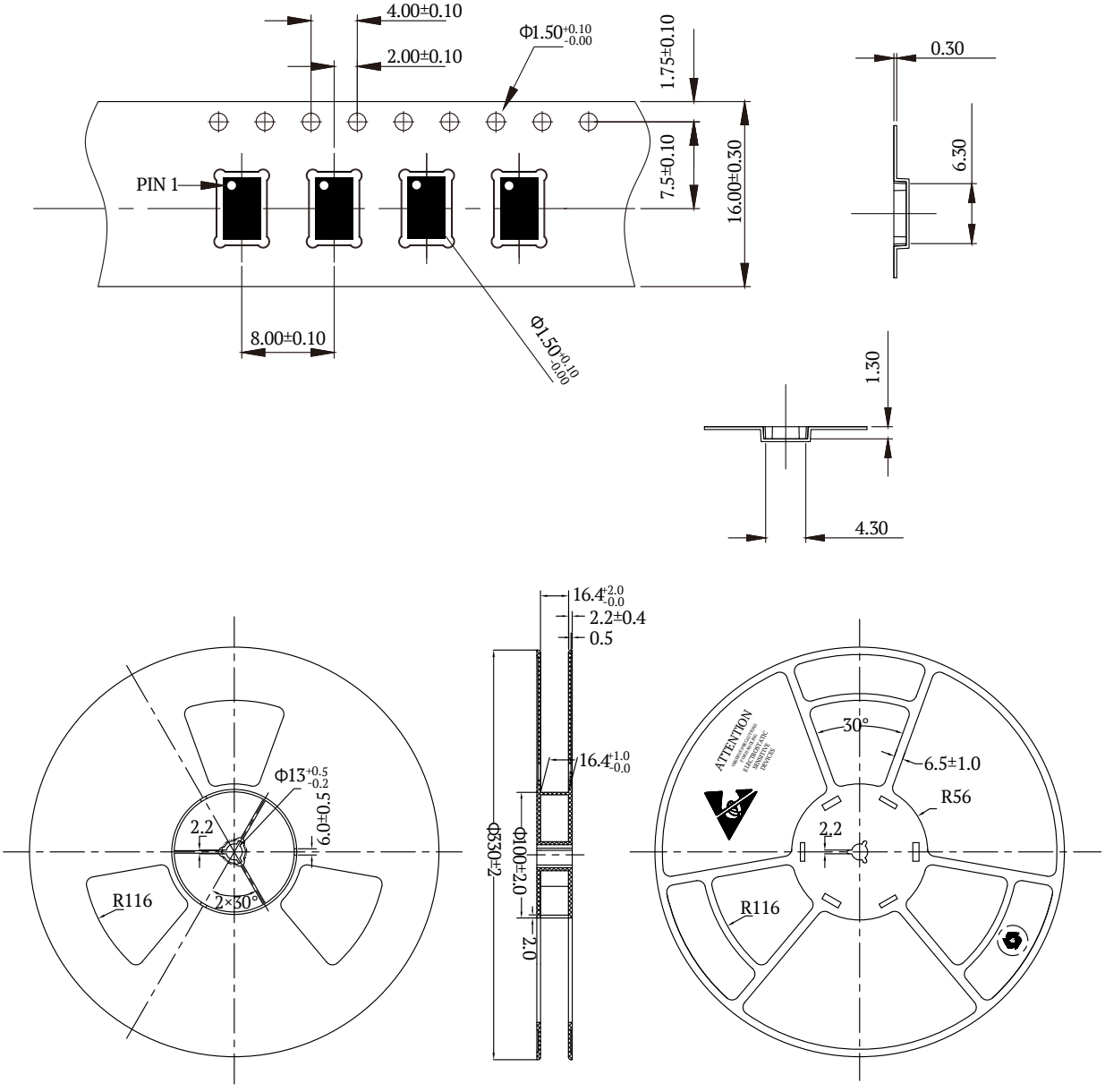


PACKING MATERIAL (TRAY)



PART NO.	PMT 0035
TRAY TYPE	4×6×1.3mm
QTY	364ea/Pcs
UNIT SIZE	mm

PACKING MATERIAL (TAPE&REEL)



NOTE:

1. Unit Size: mm
2. SPQ: 3000 PCS