3V to 17V Input, 3A Step-Down Module Regulator

DESCRIPTION

The EZ8603 is a tiny step-down DC/DC Regulator module capable of providing up to 3A output current from a 3V to 17V input supply. The output voltage can be regulated as low as 0.8V. Included in the package are the switching controllers, power FETs and inductor. Thus, only a few input and output capacitors are needed to save PCB area.

The EZ8603 uses a constant-on-time (COT) control architecture for fast transient response and easy loop compensation. To maximize efficiency at light load current, the converter can automatically enter power save mode, which only consumes 65μA (typical) quiescent current. Its 100% duty cycle operation delivers low drop -out. An internal or external soft-start and power good indicator are incorporated to simplify the power supply rail sequencing. It also features several fault protections, such as a Hiccup mode short circuit protection, overvoltage and overtemperature shutdown protection.

FEATURES

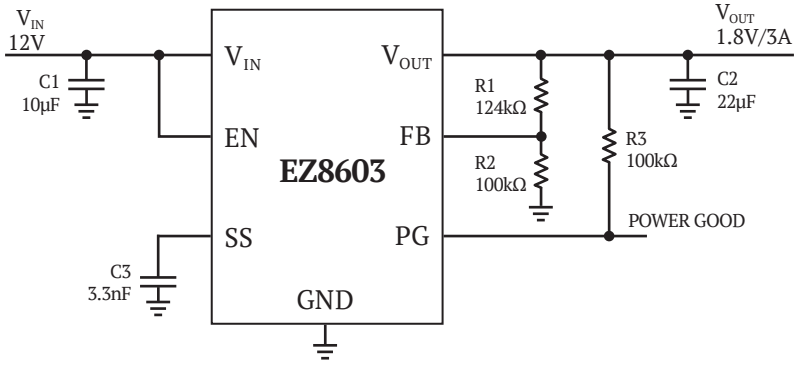
- Complete ezSiP® Power Supply
- Input Voltage Range 3V to 17V
- Output Voltage Range 0.8V to 6V
- ±1.2% Maximum Total DC Output Error over Line, Load and Temperature
- Low 65μA Quiescent Current in Power Save Mode
- 45mΩ and 20mΩ Integrated Power MOSFETs
- 2MHz Fast Switching Frequency
- Soft-Start and Power Good Indicator
- 100% Duty Cycle for Lowest Dropout
- Hiccup Mode Short Circuit Protection
- Ultra-Small 2.8mm × 3mm × 1.23mm NECP Package

APPLICATIONS

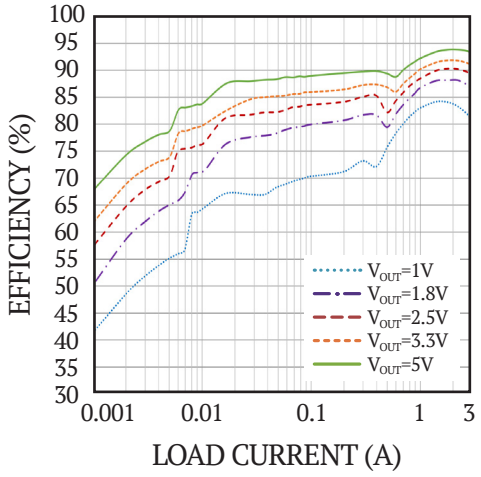
- Point-of-Load Application
- Industrial Applications
- Telecom and Networking Applications

TYPICAL APPLICATION

12V Input, 1.8V/3A Output DC/DC Regulator

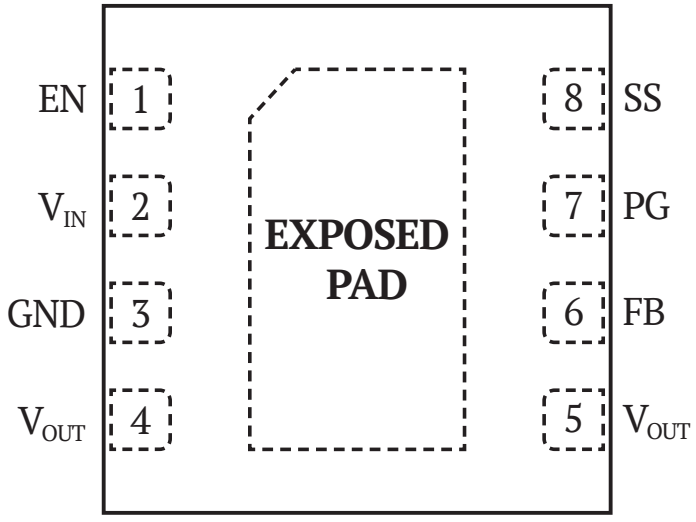


Efficiency at 12V Input Voltage



PIN CONFIGURATION AND FUNCTIONS

TOP VIEW



8-LEAD 2.8mm × 3mm × 1.23mm NECP PACKAGE
θ_{JCTOP}=10.2°C/W, θ_{JCBOT}=31.5°C/W, θ_{JA}=42.0°C/W, θ_{JB}=32.3°C/W
T_{JMAX}=125°C, Weight=0.04g

PIN#	PIN Name	PIN Description
1	EN	Device Enable Pin. To enable the device, this pin needs to be pulled high. Pulling this pin low disables the device. This pin has an internal pull-down resistor of typically 400kΩ when the device is disabled.
2	V_{IN}	Input Voltage Pin. Decouple this pin to GND with a capacitor.
3	GND	Ground Pin.
4, 5	V_{OUT}	Output Voltage Pins.
6	FB	Error Amplifier Feedback Pin. Connect this pin to the external resistor divider across the output.
7	PG	Power Good Indicator. The open drain output is pulled high by external resistor when the output voltage is within 87.5% to 112.5% of the regulation point.
8	SS	Soft Start-up Pin. An external capacitor connected to this pin sets the internal reference voltage rising time. Float this pin to use internal 1ms soft-start time.
EXPOSED PAD		The exposed thermal pad must be connected to the GND pin. Must be soldered to achieve appropriate power dissipation and mechanical reliability.

ORDER INFORMATION

PART NUMBER	FINISH	MARKING	PACKAGE TYPE	PACKING MATERIAL	MSL	TEMPERATURE RANGE
EZ8603IV#PBF	Au(RoHS)	SE	NECP	TRAY	3	-40°C to 125°C
EZ8603IV#TRPBF	Au(RoHS)	SE	NECP	TAPE&REEL	3	-40°C to 125°C

ABSOLUTE MAXIMUM RATINGS

	MIN	TYP	MAX	UNIT
Terminal Voltage				
V_{IN}	-0.3		20	V
EN, SS	-0.3		V_{IN}+0.3	V
PG, FB, V_{OUT}	-0.3		7	V
Temperatures				
Internal Operating Temperature Range	-40		125	°C
Storage Temperature Range	-55		150	°C
Peak Solder Reflow Package Body Temperature		260		°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

ESD RATINGS

HBM (Human Body Model)	2	kV
CDM (Charged Device Model)	2	kV

Note: JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process. JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

RECOMMENDED OPERATING CONDITIONS

	MIN	TYP	MAX	UNIT
Supply Input Voltage	3		17	V
Output Voltage	0.8		6	V
Output Current	0		3	A
Power Good Pull-up Resistor Voltage			6	V
Junction Operating Temperature Range	-40		125	°C

ELECTRICAL CHARACTERISTICS

The Y denotes the specifications which apply over Full Temperature Range (FTR) (Note 1). Typical values are at T_A = 25°C, V_{IN} = V_{EN} = 12V unless otherwise noted. The values are guaranteed by test, design or statistical correlation.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	FTR
Input DC Voltage	V_{IN}		3		17	V	Y
Output Voltage Range	$V_{OUT(RANGE)}$		0.8		6	V	Y
Output Voltage, Total Variation with Line and Load	$V_{OUT(DC)}$	C_{IN} = 10µF, C_{OUT} = 22µF Ceramic R_{TOP} = 124kΩ, R_{BOT} = 100kΩ, V_{IN} = 3V to 17V, I_{OUT}= 1A to 3A	1.778	1.8	1.822	V	Y
Undervoltage Lockout	$V_{IN\ UVLO}$	V_{IN} Falling	2.5	2.6	2.7	V	
UVLO Hysteresis	$V_{UVLO\ HYS}$			200		mV	
Quiescent Current	I_Q	V_{EN} = High, V_{IN} = 12V, V_{OUT} = 1.8V, V_{FB} = 1.0V		65		µA	
Shutdown Current	I_{SHDN}	V_{EN} = Low		6		µA	
EN Rising Threshold	V_{ENR}		1.25			V	
EN Falling Threshold	V_{ENF}				0.5	V	
EN Leakage Current	$I_{LKG(EN)}$	V_{EN} = High		0.1	1	µA	
SS Pin Source Current	I_{SS}			2.5		µA	
Internal Soft Start Time	t_{SS}	Float SS pin, Time from EN High to 95% of V_{OUT} Nominal		1		ms	
Voltage at FB Pin	V_{FB}	I_{OUT} = 1A, V_{OUT} = 1.8V, -40°C < T_J < 125°C	792	800	808	mV	Y
Current at FB Pin	I_{FB}		-30		30	nA	
Load Regulation	$\Delta V_{OUT}/V_{OUT}$	I_{OUT} = 0A to 3A, V_{OUT} = 1.8V		0.15		%/A	
Line Regulation	$\Delta V_{OUT}/V_{OUT}$	I_{OUT} = 1A, V_{OUT} = 1.8V, V_{IN} from 3V to 17V		0.02		%/V	
Output Continuous Current Range	$I_{OUT(DC)}$	V_{IN} = 12V, V_{OUT} = 1.8V (Note 2)			3	A	
Output Ripple Voltage	$V_{OUT(AC)}$	C_{OUT} = 22µF Ceramic V_{IN} = 12V, V_{OUT} = 1.8V, I_{OUT} = 0.5A		15		mV	
Output Discharge Resistor	R_{DIS}	EN = Low, V_{OUT} = 1.8V		280		Ω	
Power Good Trip Level	V_{PGUV}	V_{FB} Ramping Negative, V_{FB} With Respect to Set Output	84	87.5	91	%	
	V_{PGOV}	V_{FB} Ramping Positive, V_{FB} With Respect to Set Output	109	112.5	116	%	
PG Pin Leakage Current	I_{PG}	V_{PG} = 5V			1	µA	
PG Voltage Low	V_{PG_LOW}	I_{PG} = 2mA		0.02	0.3	V	
High-side FET On-Resistance	R_{HFET}	V_{IN} = 12V, V_{OUT} = 1.8V		45		mΩ	
Low-side FET On-Resistance	R_{LFET}	V_{IN} = 12V, V_{OUT} = 1.8V		20		mΩ	

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	FTR
High-side FET Current Limit	I_{LIM_PK}	V_{IN} = 12V, V_{OUT} = 1.8V		5		A	
Low-side FET Current Limit	I_{LIM_VALLEY}	V_{IN} = 12V, V_{OUT} = 1.8V		4		A	
Dropout Resistance	R_{DP}	100% mode, V_{IN} = 3V, T_A = 25°C		90		mΩ	
Switching Frequency	F_S	I_{OUT} = 1A		2		MHz	

Note 1: The EZ8603 is tested under pulsed load conditions such that $T_J \approx T_A$. The EZ8603IV is guaranteed over the full -40°C to 125°C internal operating temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

Note 2: See output current derating curves for different V_{IN}, V_{OUT} and T_A.

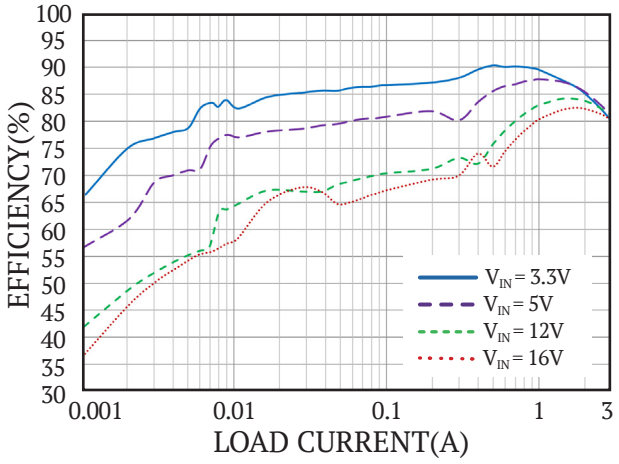
Note 3: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. The over-temperature protection is active when the junction temperature exceeds 150°C. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

REVISION HISTORY

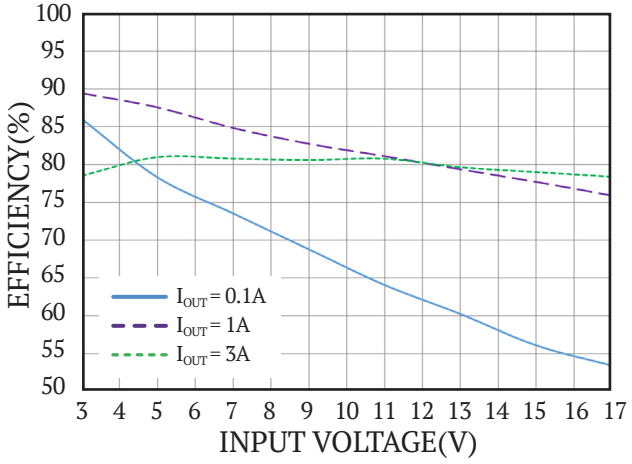
REV.	DATE	CHANGES
D	Jun 2026	1. Page 17 Package Outline Drawings Update. 2. Page 1-3 Package Name Changed from LQFN to NECP.
C	Jul 2025	Page 17-19 Packing Drawings Update.
B	Aug 2023	1. Order Information Added 2. TAPE&REEL Drawing Information Added
A	Mar 2023	Initial Release

ELECTRICAL CHARACTERISTICS

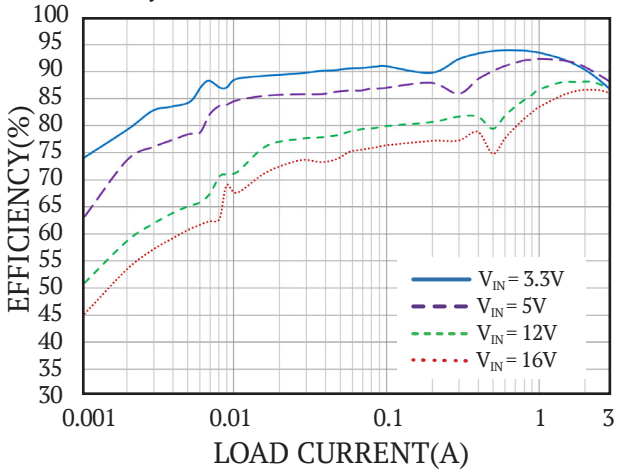
Efficiency vs Load Current From 1V Output



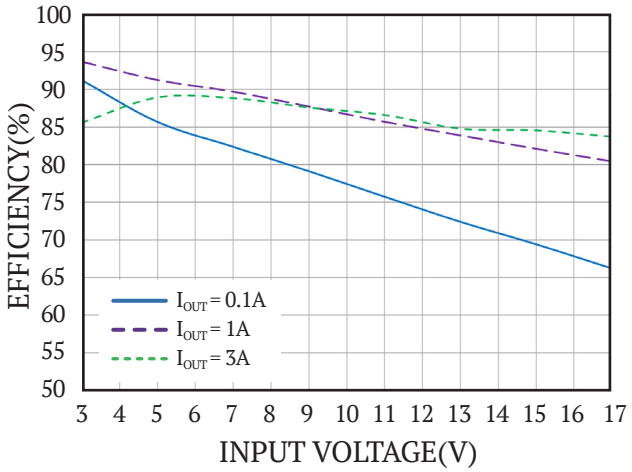
Efficiency vs Input Voltage From 1V Output



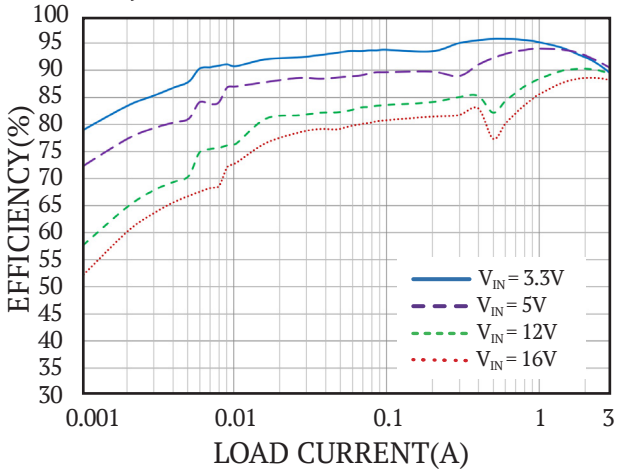
Efficiency vs Load Current From 1.8V Output



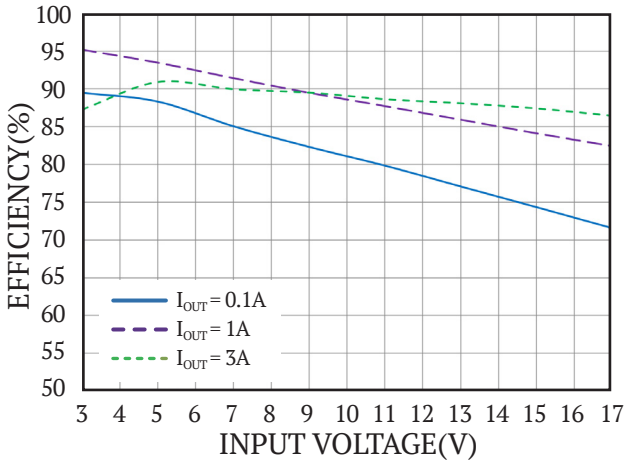
Efficiency vs Input Voltage From 1.8V Output



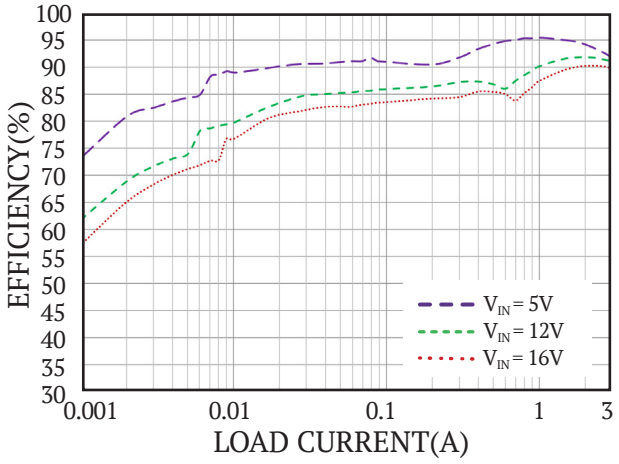
Efficiency vs Load Current From 2.5V Output



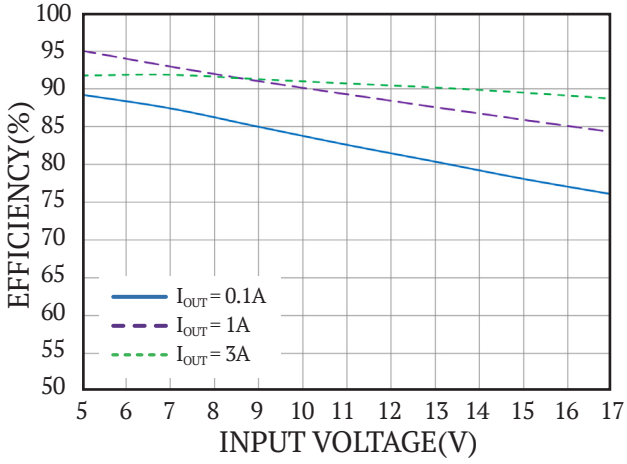
Efficiency vs Input Voltage From 2.5V Output



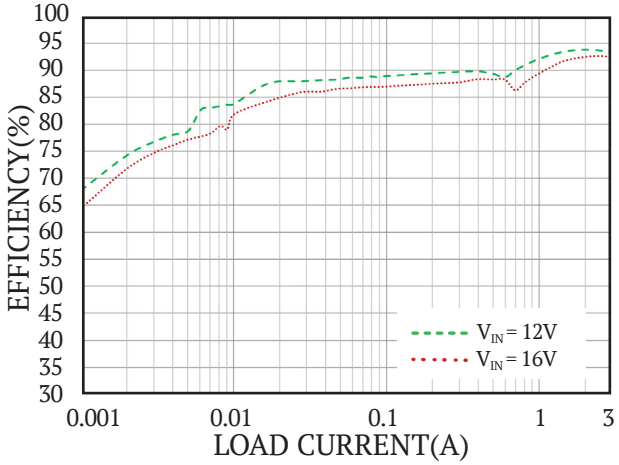
Efficiency vs Load Current From 3.3V Output



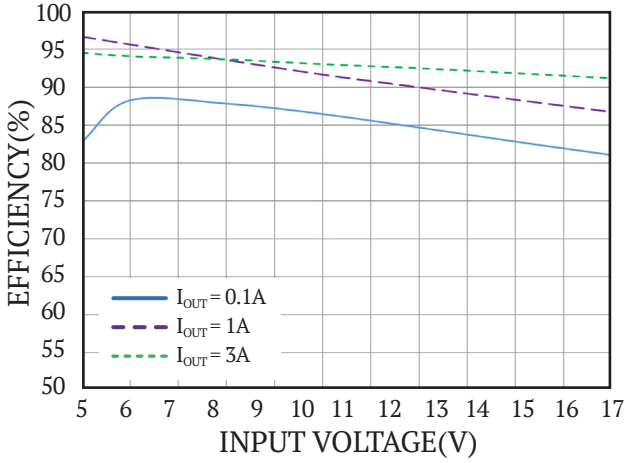
Efficiency vs Input Voltage From 3.3V Output



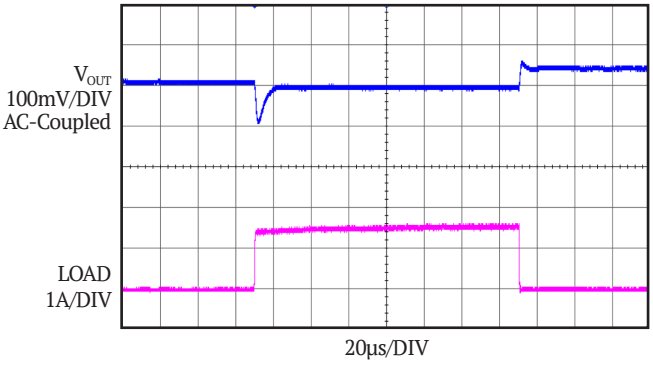
Efficiency vs Load Current From 5V Output



Efficiency vs Input Voltage From 5V Output

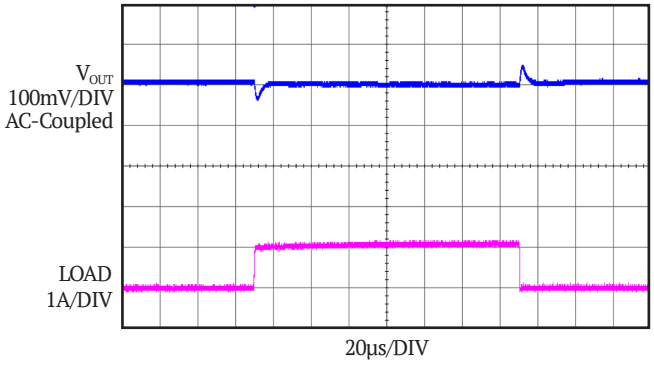


LOAD-STEP(PFM)



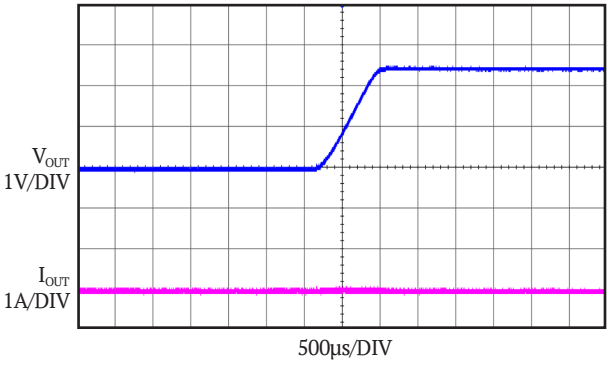
V_{IN}=5V, V_{OUT}=2.5V
0-1.5 LOAD STEP
C_{OUT}=10μF×2 CERAMIC CAP

LOAD-STEP(CCM)



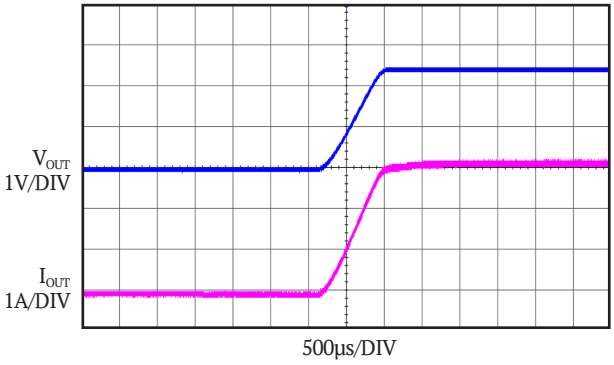
V_{IN}=5V, V_{OUT}=2.5V
0.5-1.5 LOAD STEP
C_{OUT}=10μF×2 CERAMIC CAP

Start-up with No Load Current



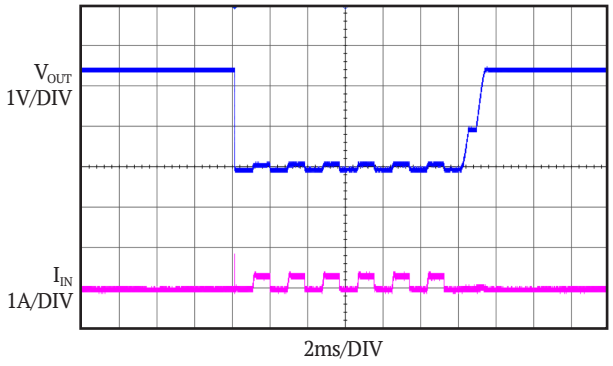
V_{IN}= 5V, V_{OUT}= 2.5V
USE EN PIN TO CONTROL START-UP
I_{OUT}= 0A, C_{OUT}= 10μF×2 CERAMIC CAP

Start-up with 3A Load Current



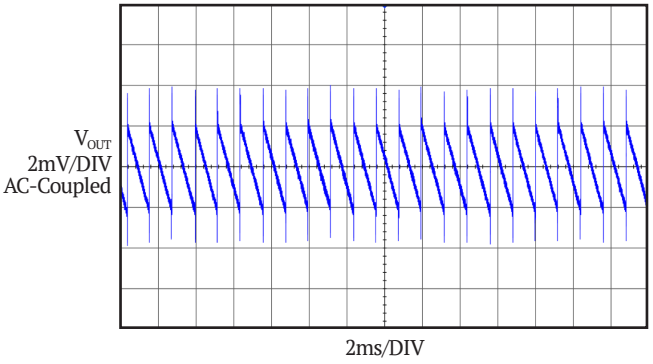
V_{IN}= 5V, V_{OUT}= 2.5V
USE EN PIN TO CONTROL START-UP
I_{OUT}= 1.5A, C_{OUT}= 10μF×2 CERAMIC CAP

Short Circuit Protecttion



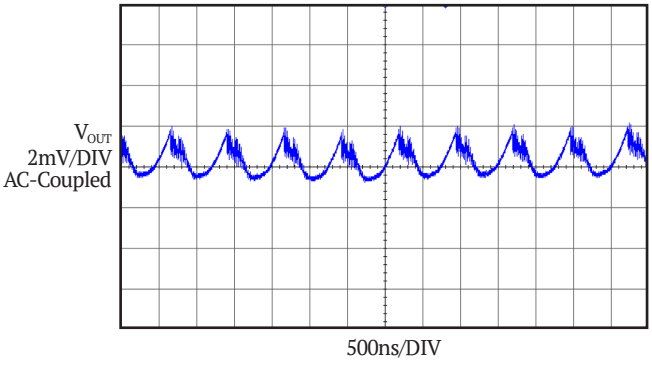
V_{IN} = 3.3V, V_{OUT} = 2.5V
I_{OUT} = 0A
C_{OUT} = 10μF×2 CERAMIC CAP

Output Ripple(PFM)



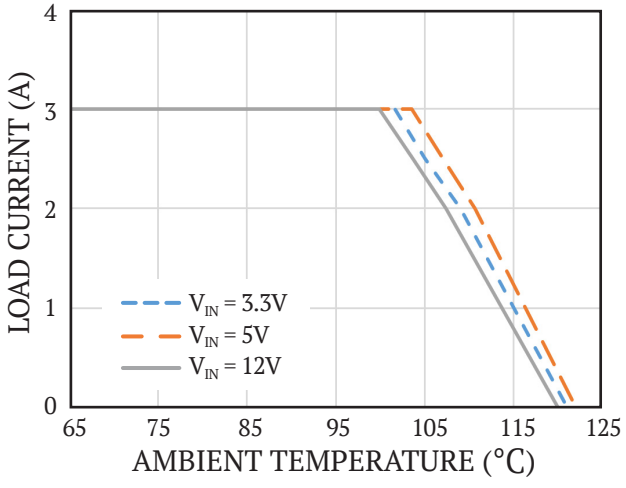
V_{IN} = 3.3V, V_{OUT}=2.5V, I_{OUT} = 0A
C_{OUT} = 10μF×2 CERAMIC CAP

Output Ripple(CCM)

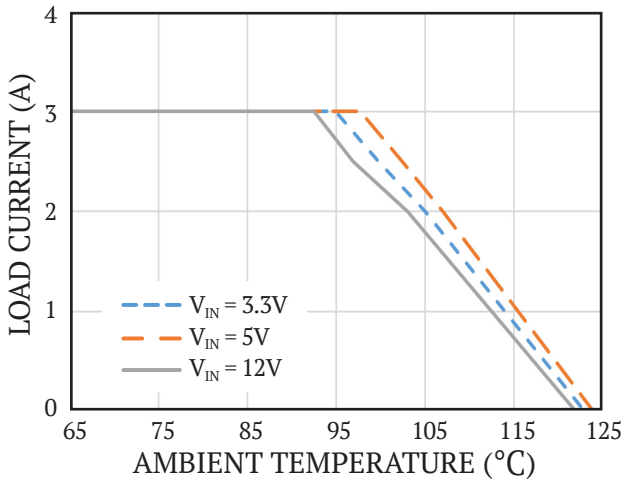


V_{IN}=3.3V, V_{OUT}=2.5V, I_{OUT} = 3A
C_{OUT}=10μF×2 CERAMIC CAP

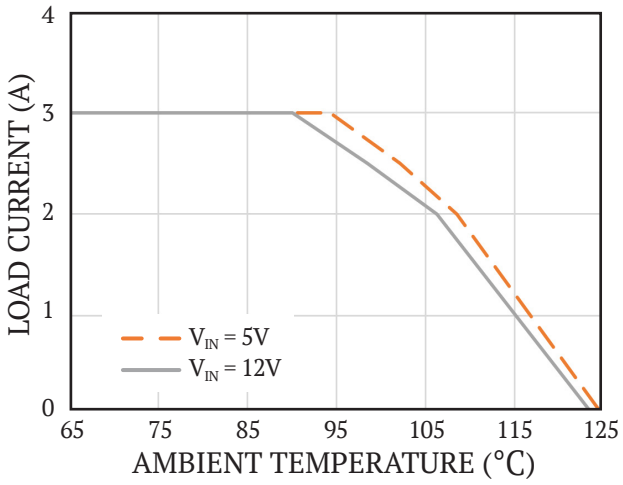
Derating Curve: V_{OUT}=1V



Derating Curve: V_{OUT}=1.8V



Derating Curve: V_{OUT}=3.3V



BLOCK DIAGRAM

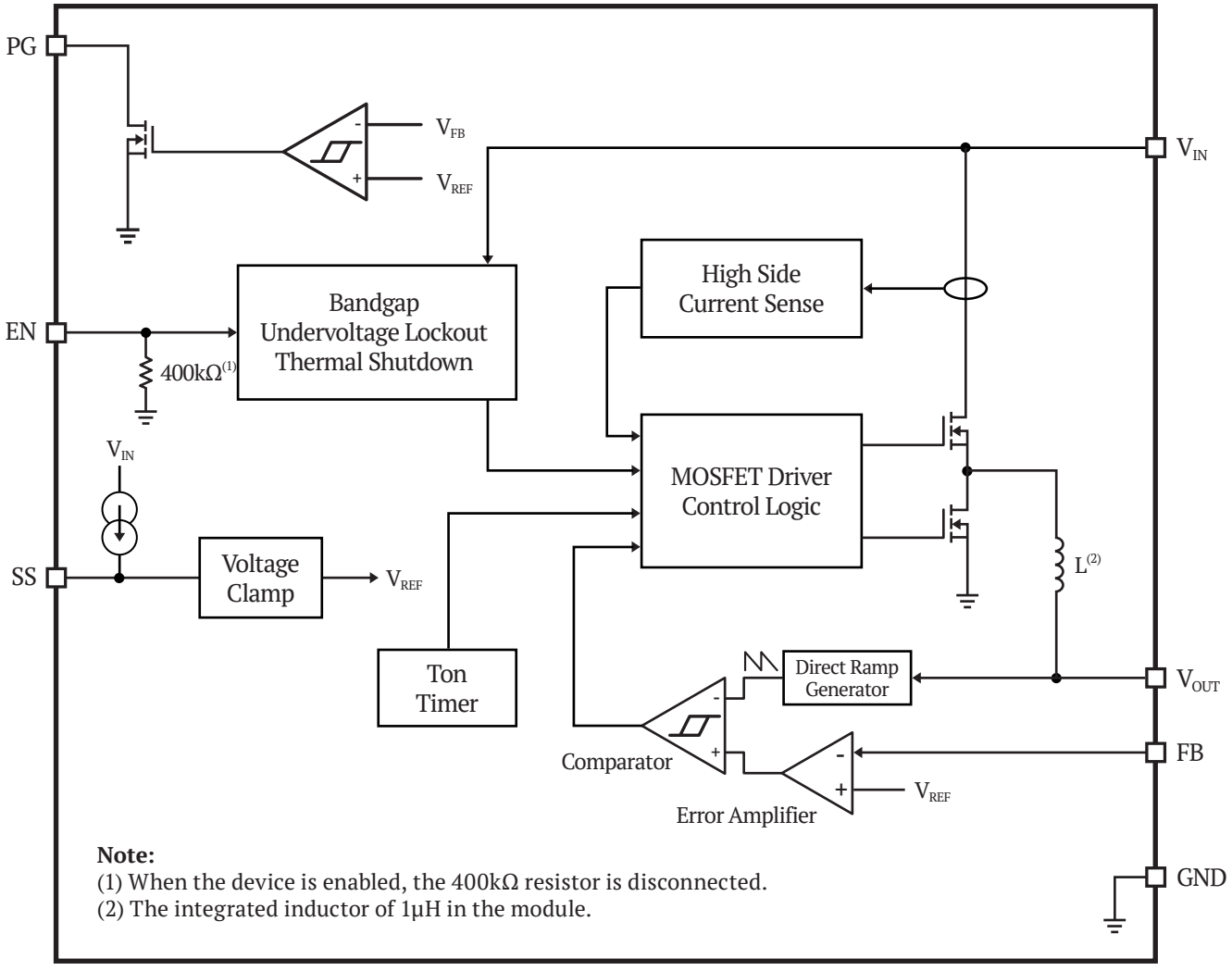


Figure 1 Simplified EZ8603 Internal Function Block Diagram

OPERATION

POWER MODULE DESCRIPTION

The EZ8603 ezSiP® Power Module is a high-performance single output standalone non-isolated switching mode DC/DC power supply. It can provide a single 3A output with a few external input and output capacitors. This module provides a precisely regulated output voltage programmable via an external resistor divider. The typical application schematic is shown in Figure 4.

The EZ8603 ezSiP® Power Module has an integrated constant on-time (COT) regulator and built-in power MOSFETs, and power inductors. For medium to heavy load conditions, the converter operates in Pulse Width Modulation Mode (PWM) with 2MHz switching frequency. At light loads, the switching frequency will be reduced and the quiescent current of the converter will also be minimized to achieve high efficiency. See the Applications Information section.

During a load transient event, with the help of COT control architecture, the EZ8603 ezSiP® Power Module can turn on its high-side power switch immediately to achieve a very good transient performance with sufficient stability margins over a wide range of output capacitors, even with all ceramic output capacitors.

Pulling the EN pin below 0.5V forces the regulator into a shutdown state. Pulling the EN pin above 1.25V to enable the EZ8603. The internal or external soft-start can be used for programming the output voltage soft-start ramp during the start-up. See the Application Information section.

APPLICATIONS INFORMATION

The typical EZ8603 application circuit is shown in Figure 4. External component selection is primarily determined by the maximum load current and output voltage.

OUTPUT VOLTAGE PROGRAMMING

The EZ8603 has an internal 0.8V reference voltage. The output voltage is set by the two resistors between the ground and V_{OUT}. The output voltage can be calculated by the function:

$$V_{OUT} = 0.8V \cdot (1 + \frac{R_A}{R_B})$$

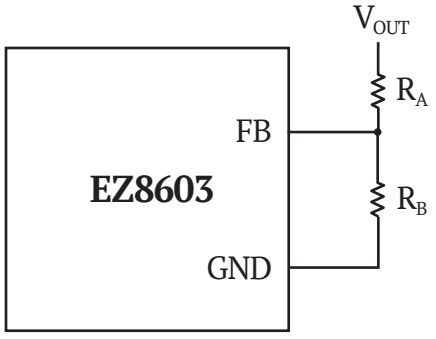


Figure 2 Output Voltage Programming Diagram

INPUT CAPACITORS

The EZ8603 should be connected to a low AC impedance DC source. Also input ceramic capacitors are needed for the RMS input ripple current rating. A typical 10μF ceramics capacitor is a good choice with RMS ripple current ratings of ~1A.

A 47μF to 100μF aluminum electrolytic bulk capacitor can be added only if the input source impedance is compromised by long inductive leads, traces or not enough source capacitance.

For a buck converter, the switching duty cycle can be estimated as:

$$D = \frac{V_{OUT}}{V_{IN}}$$

Without considering the inductor ripple current, for each output, the RMS current of the input capacitor can be estimated as:

$$I_{CIN(RMS)} = \frac{I_{OUT(MAX)}}{\eta\%} \cdot \sqrt{D \cdot (1 - D)}$$

In the previous equation, η% is the estimated efficiency of the power module.

OUTPUT CAPACITORS

The EZ8603 is designed for low output voltage ripple noise. To meet the output voltage ripple and transient requirements, the output capacitor C_{OUT} can be a low ESR tantalum capacitor, low ESR Polymer capacitor or even all ceramic capacitors.

The typical output capacitance range is from 22μF to 100μF. Additional output filtering may be required by the system designer if further reduction of output ripple or dynamic transient spikes is required.

PFM OPERATION

The EZ8603's low output ripple and high efficiency at intermediate currents are achieved with Pulse Frequency Modulation (PFM). In PFM operation, the low side Synchronous rectifier MOSFET turns off to prevent the inductor current go negative during the light load condition. If the load current is further reduced, the control circuit will start to reduce switching frequency to further enhance efficiency. The switching frequency could be lower than audible frequency area under deep light load condition.

SOFT-START

The EZ8603 incorporates an internal soft-start to reduce the voltage and current stress during the start-up. The internal soft-start is set to approximately 1ms. Customer can also adjust the output voltage rising slope by an external capacitor connected to the SS pin.

The EZ8603 is capable of monotonically starting into a pre-biased output voltage. It starts to switching operation with the applied bias voltage and ramps to output voltage to its nominal value.

ENABLE AND DISABLE

The EZ8603 is enabled by setting the EN pin to a logic high with the threshold of 1.25V maximum. When the EN pin voltage is lower than 0.5V, the EZ8603 enters shutdown mode. In shutdown mode, the internal power switches and most control circuitry are turned off, reducing the input current to typically 6μA. An internal 400kΩ pull-down resistor is connected between the EN

pin and the ground when the EN pin is low.

POWER GOOD

The PG pin is open drain pin that can be used to monitor valid output voltage regulation. A resistor can be pulled up to a particular supply voltage no greater than 6V for monitoring. PG remains low until the FB pin is within 87.5% to 112.5% of the final regulation voltage.
The PG pin can be used for sequencing of multiple rails by connecting to the EN pin of other converters. The PG pin can be left floating or connected to ground if not used.

LOW DROPOUT MODE

When the input voltage decreases, the switching frequency decreases, the on-time is increased to maintain the regulation. As the input voltage drops further, the top MOSFET is turned on for 100% of the cycle to allow the output voltage to be very close to the input voltage.

OVERCURRENT PROTECTION

The EZ8603 has a cycle-by-cycle peak and valley current mode over current protection (OCP) in a short circuit. If the inductor current reaches the peak current limit, The top MOSFET will turn off immediately and turn on the bottom MOSFET to ramp down the inductor current. The top MOSFET will keep off until the current returns back to a safe level. The default valley current limit is set to around 4A to guarantee a DC output current higher than 3A.

OUTPUT UNDER VOLTAGE PROTECTION (UVP)

If the output voltage is less than 35% of the set voltage point for approximately 4μs occurring when the output short circuit or the load current is much heavier than the maximum current capacity, the output under voltage protection (UVP) will be triggered, and the device will enter into Hiccup protection mode. The typical Hiccup on time is 1ms, and the Hiccup off time is 1ms. If the output fault conditions are removed, the device will go back to normal operation in the nearest Hiccup on time.

OUTPUT OVER VOLTAGE PROTECTION (OVP)

If the DC output voltage is about 5% over the regulation level, the bottom MOSFET will keeps on until the inductor current ramps down around zero. Then both top MOSFET and bottom MOSFET will turn off and enter into stand-by mode.

OVER TEMPERATURE PROTECTION (OTP)

The EZ8603 incorporates an over temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. The device will shut down when the junction temperature exceeds 150°C. Once the junction temperature cools down by approximately 10°C, the device will resume normal operation after a complete soft-start cycle.

OUTPUT DISCHARGE FUNCTION

The EZ8603 discharges the output voltage when the converter shuts down from VIN or EN, or thermal shutdown, so that output voltage can be discharged in a minimal time, even load current is zero. The discharging FET which in parallel with the low-side synchronous rectifier turns on after the low-side synchronous rectifier turns off when shut down logic is triggered. The output discharge resistor is typically 280Ω under room temperature. Note that the discharge FET is not active beyond these shutdown conditions.

STABILITY COMPENSATION

The EZ8603 module has already been internally compensated for all output voltages.

LAYOUT CHECKLIST/EXAMPLE

The high integration of EZ8603 makes the PCB board layout very simple and easy. However, to optimize its electrical and thermal performance, some layout considerations are still necessary.

- Use large PCB copper areas for high current paths, including V_{IN}, GND, and V_{OUT}. It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the V_{IN}, GND and V_{OUT} pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the unit.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for inter-connection between top layer and other power layers.
- Do not put via directly on the pad, unless they are capped or plated over.
- Bring out test points on the signal pins for monitoring.

Figure 3 gives a good example of the recommended layout.

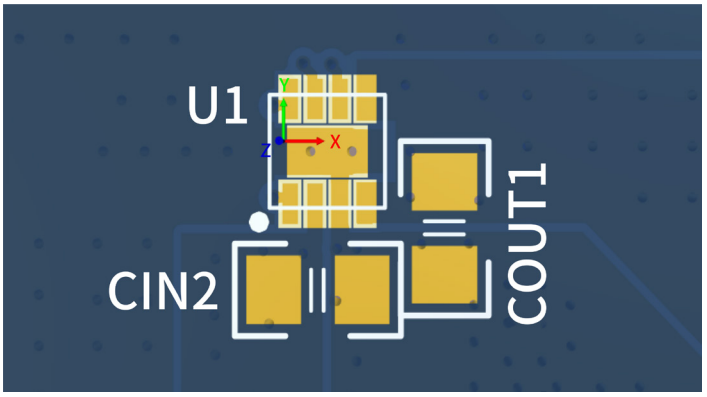


Figure 3 Recommended Layout

TYPICAL APPLICATIONS

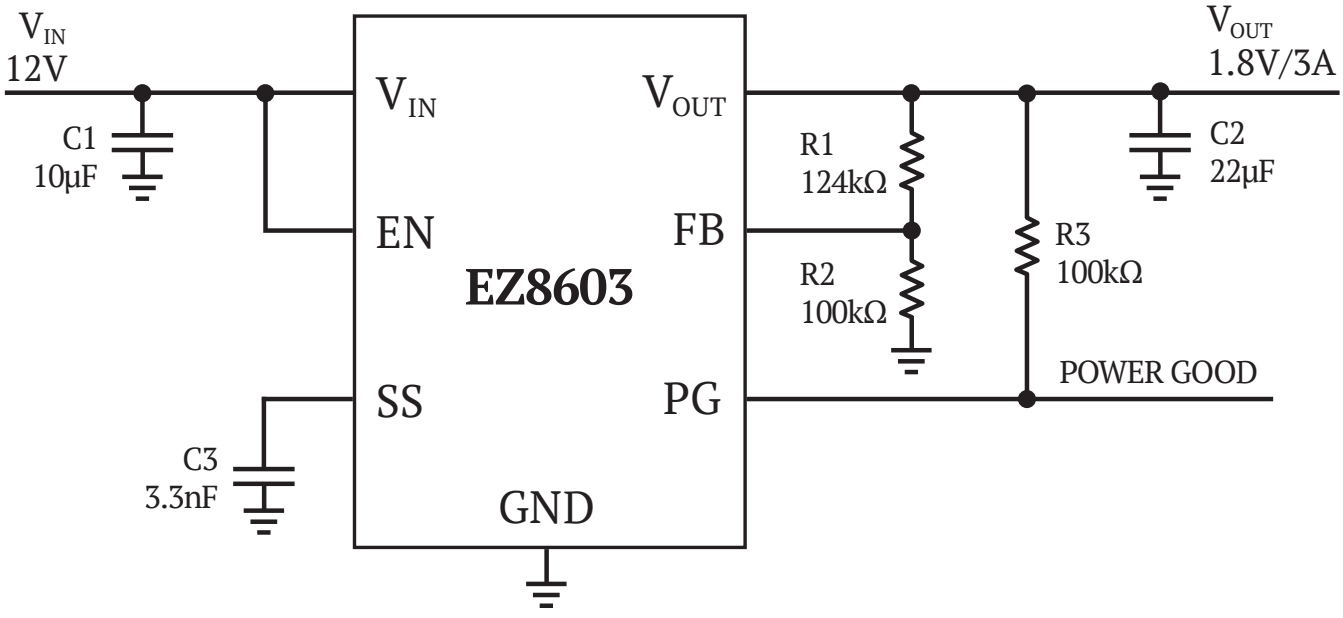


Figure 4 Typical 12V Input, 1.8V at 3A Output Design

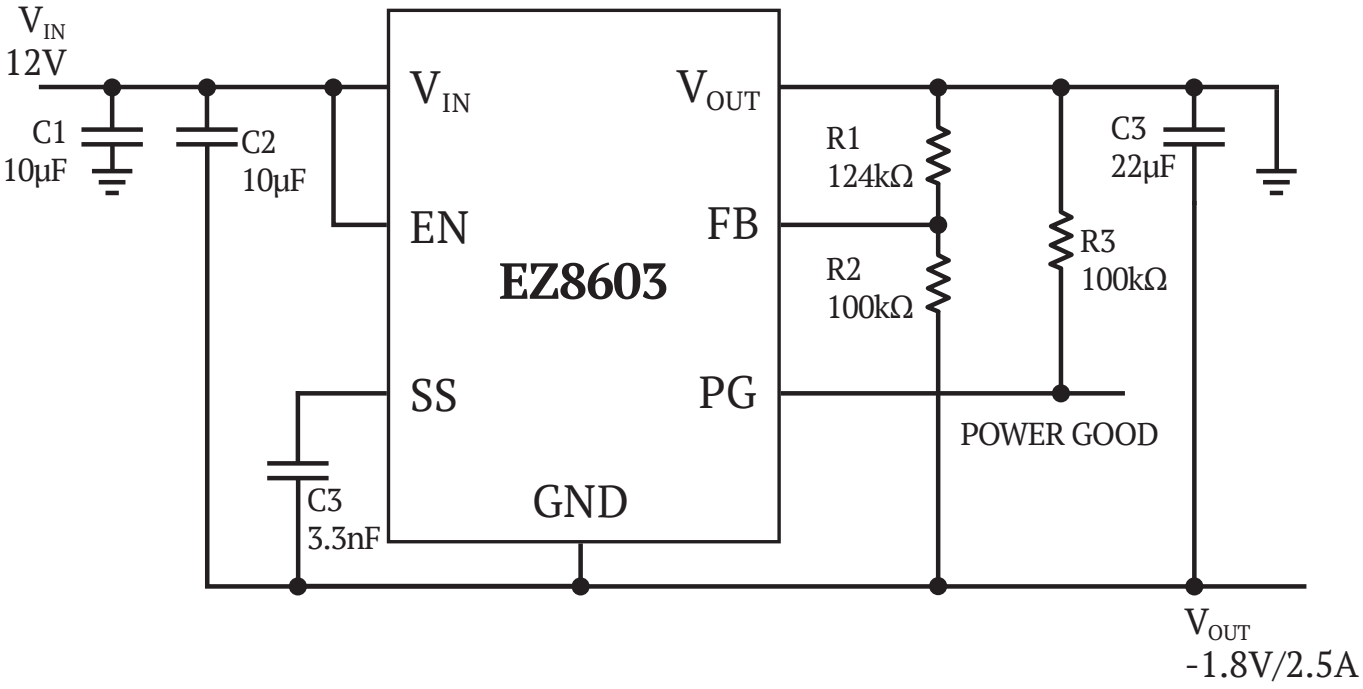
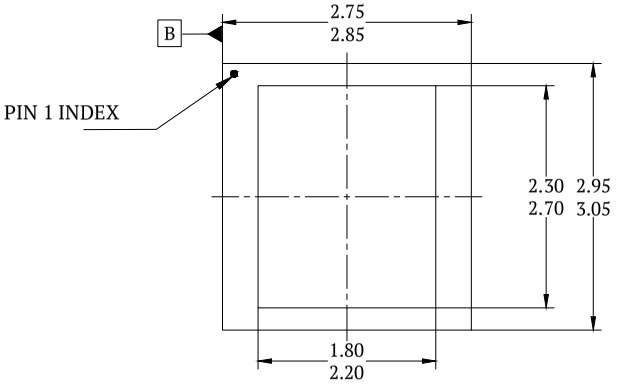


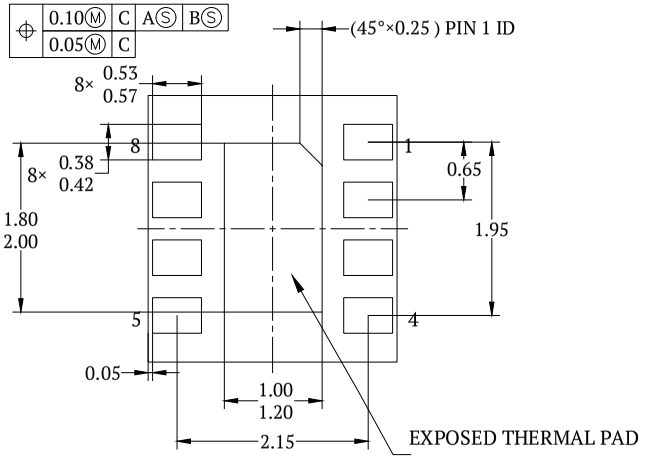
Figure 5 Typical 12V Input, -1.8V at 2.5A Output Design

PACKAGE OUTLINE DRAWING

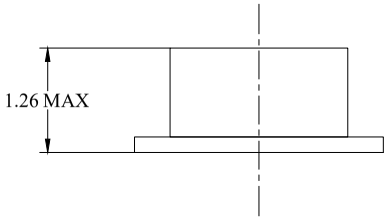
NECP PACKAGE
8-LEAD 2.80mm × 3.00mm × 1.23mm
POD-0055-A3
Unit:mm



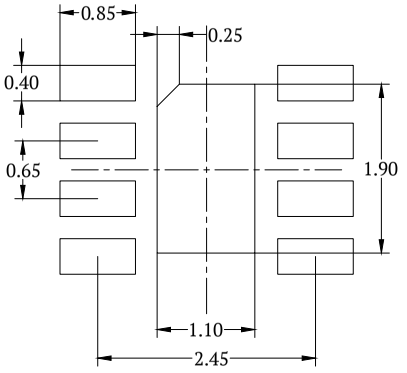
TOP VIEW



BOTTOM VIEW

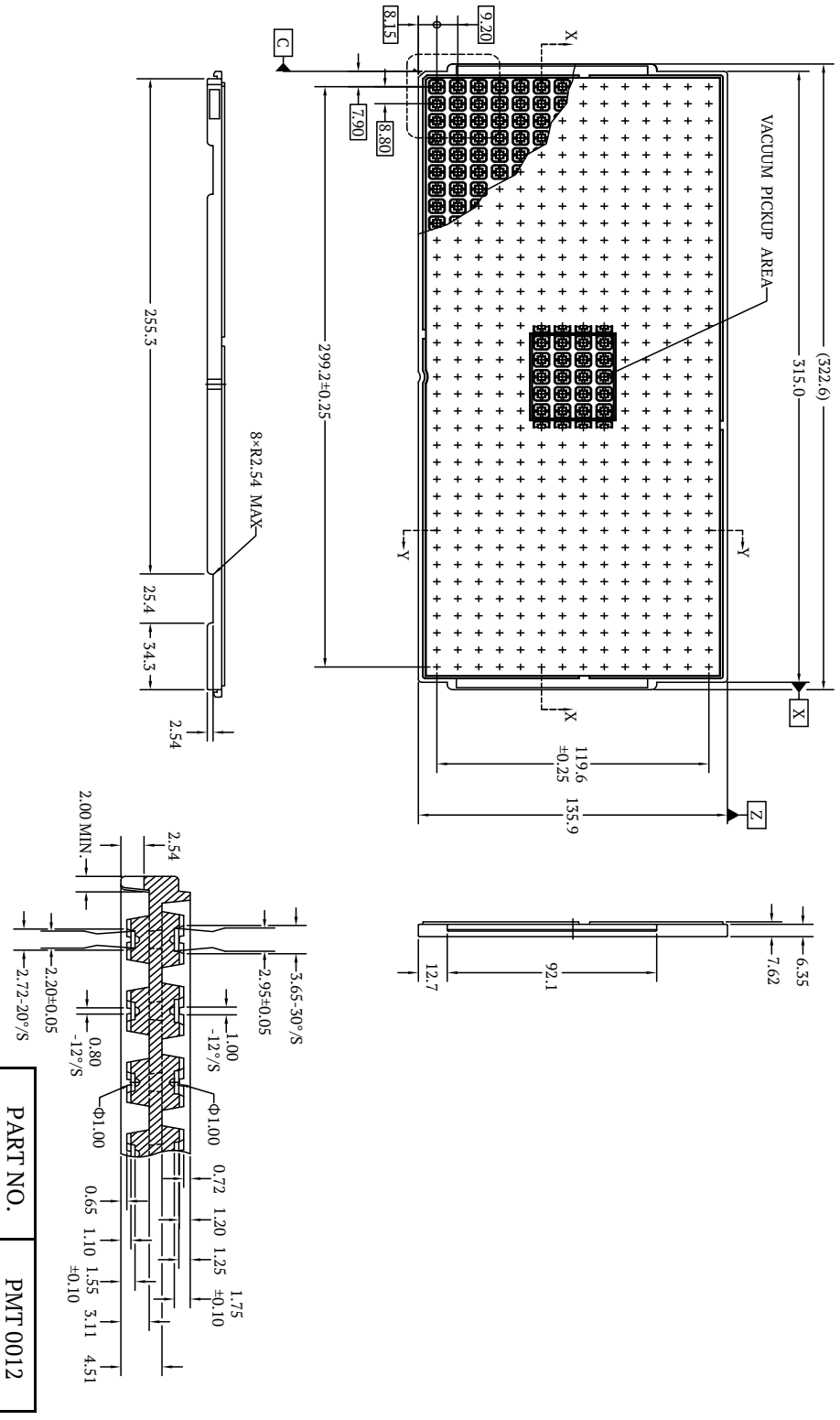


SIDE VIEW



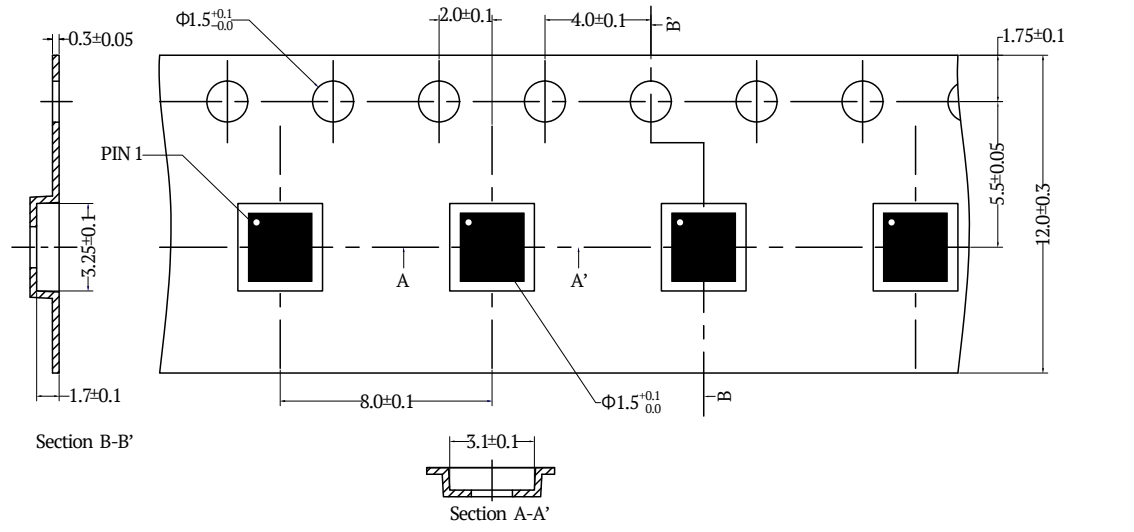
SUGGESTED PCB LAYOUT TOP VIEW

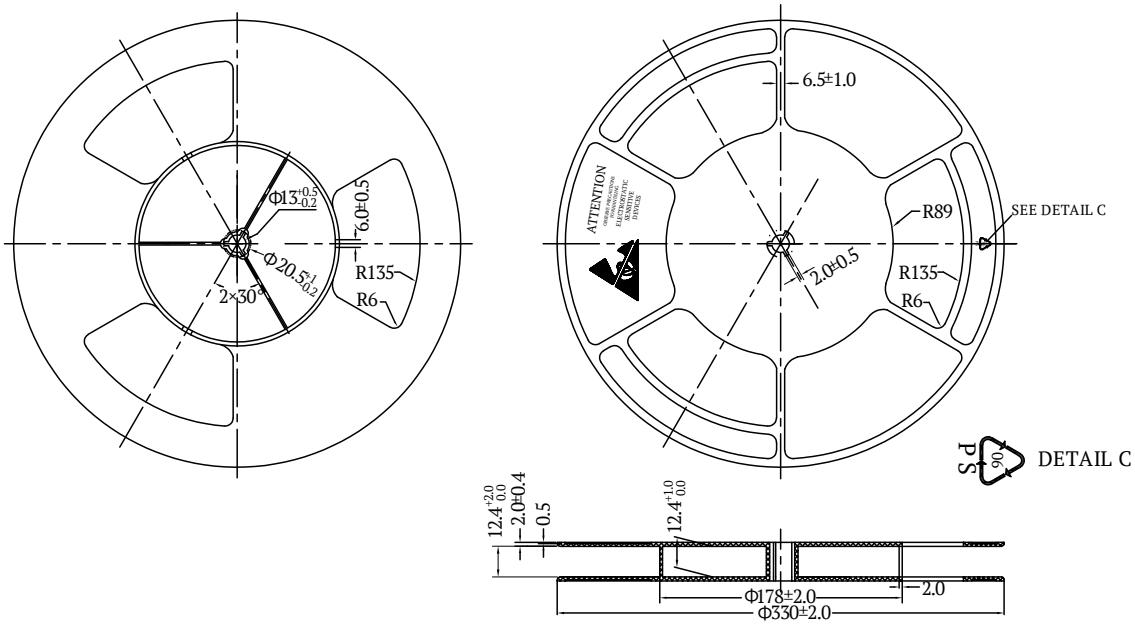
PACKING MATERIAL (TRAY)



PART NO.	PMT 0012
TRAY TYPE	2.95×3.15×1.93mm
QTY	490ea/Pcs
UNIT SIZE	mm

PACKING MATERIAL (TAPE & REEL)





NOTE:

1. Unit Size: mm
2. SPQ: 3000 PCS